Single Electron Transistors with Sidewall Depletion Gates on a Silicon-On-Insulator Quantum Wire

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For practical application to multi-functional nanoelectronic devices, single electron transistors (SETs) should have controllable and reproducible characteristics. For high temperature operation, recently proposed SET structures have depended on somewhat contingent phenomena such as unintentional potential barriers in quantum wires [1], e-beam irregularity [2] or randomly distributed nanocrystal arrays [3], so that their device characteristics couldn't be predicted. In this work, SETs with sidewall depletion gates on a silicon-on-insulator (SOI) quantum wire have been fabricated by the combination of conventional lithography and VLSI technology, and their properties were investigated.

Figure 1 shows a schematic of the fabricated device. Inversion layer in a p-type 45nm-thick SOI quantum wire channel is formed by the back gate bias (V_{BG}), and two tunnel junctions are formed by the sidewall depletion gate bias (V_{SG}). The charge of electrically formed quantum dot is controlled by the control gate bias (V_{CG}). A uniform 30 nm-wide SOI quantum wire was formed by sidewall patterning method [4] as shown in Fig. 2(a), which effectively suppressed unintentional potential barriers. Figure 2(b) and 2(c) show the n-type doped polycrystalline silicon sidewall gates on Si wire, which were formed by the sequential LPCVD and the reactive ion etching of polycrystalline silicon on nitride groove. The separation between two sidewall gates (S_{SG}) was designed to be 37 nm (SET1) and 185 nm (SET2), for the high temperature operation and high voltage gain, respectively. Sidewall depletion gate structure has the merit in that it can implement a feature size smaller than the limit of e-beam lithography [5].

Figure 3 shows the control gate dependence of the drain current and the differential conductance of SET1 at 77 K. Clear multiple Coulomb oscillation peaks are obtained with the period (ΔV_{CG}) of 600 mV. This characteristic is superior to the recently published Si based high temperature SETs [2, 6] in that many peaks are observed at 77K, and I_{ON}/I_{OFF} value is maintained as the control gate voltage increases. Gate capacitance of 0.27 aF extracted from ΔV_{CG} is consistent with that of 0.24 aF estimated from the device geometry. Moreover, ΔV_{CG} is constant as V_{CG} increases. These characteristics stem from the strong controllability of tunnel barriers by V_{SG}, which can be attributed to the 3-dimensional structure of the sidewall depletion gate wrapping Si channel. This is confirmed by 3-dimensional device simulation, as shown in Fig. 4. The size of electrostatically defined quantum dot is invariant in sweeping V_{CG}. Considering that, in many cases of previous reports, electrically formed quantum dots were too sensitive to gate bias conditions to maintain the reliable multiple switching performance and showed just a small number of peaks only in a subthreshold region [5, 7], the fabricated SETs are much improved and comparable to SETs by physically formed quantum dot [6]. Figure 5 shows the drain voltage dependence of the drain current of SET1 at 77 K. Coulomb gap is clear and modulated by V_{CG}. Maximum gap was about 20mV. This suggests an extremely low voltage gain, because quantum dot is weakly coupled to the control gate.

In the case of SET2 with S_{SG} of 185 nm, the area of quantum dot increases, so that the control gate capacitance and the voltage gain increase. Figure 6 shows the drain current contour of SET2 at 15 K. Clear rhombus shape and high voltage gain of 1.3 are observed. Extracted capacitances are: control gate capacitance (C_{CG})=2.13 aF, drain junction capacitance (C_D)=1.64 aF, source junction capacitance (C_S)=1.42 aF, and total capacitance (C_T)=8 aF.

In summary, reliable operation of Si based SETs fabricated by conventional VLSI technology was successfully demonstrated at 77K. Improving the performance of the suggested SETs will make the designable and reproducible high temperature SETs possible.

References

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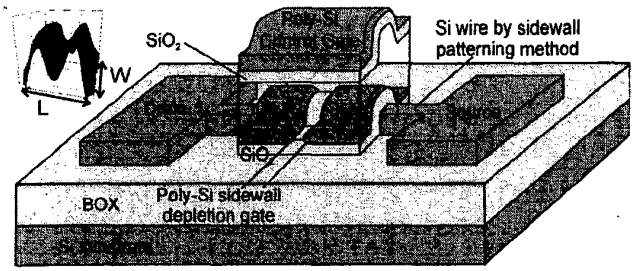

FIG. 1. Schematic diagram of the fabricated SET. Starting material was a 45nm thick SOI film. The inset shows the electron potential profile in SOI wire calculated by 3-dimensional device simulation.

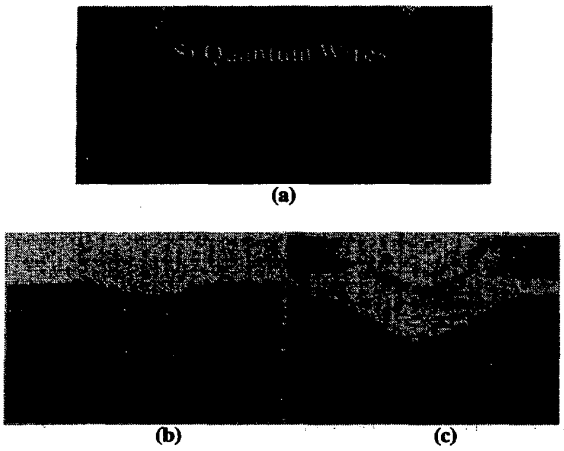

FIG. 2. (a) SEM image of Si wire formed by sidewall patterning method after the gate oxidation. Final line width was 23 nm. (b) SEM image of polycrystalline silicon sidewall depletion gates of SET1 (S_{SG}=37 nm). (c) SEM image of polycrystalline silicon sidewall depletion gates of SET2 (S_{SG}=185 nm).

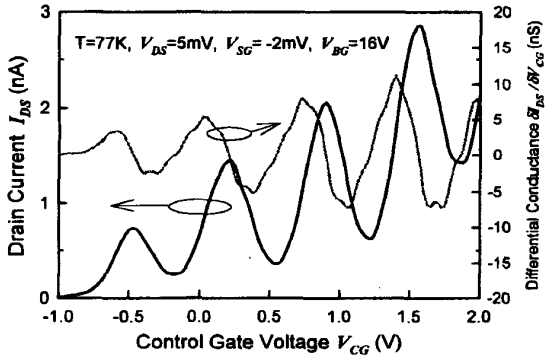

FIG. 3. Control gate dependence of the drain current and the differential conductance of SET1 at 77 K. Multiple Coulomb oscillation peaks are clearly observed. Oscillation period (ΔV_{CG}) is 600mV, which corresponds to the control gate capacitance (C_{CG}) of 0.27 aF. ΔV_{CG} is constant as V_{CG} increases.

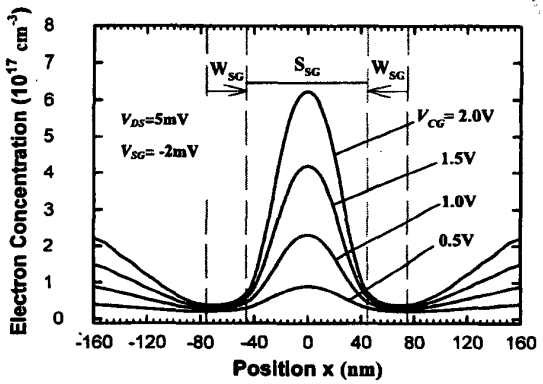

FIG. 4. Electron concentration along an SOI wire length direction at 7nm depth beneath Si/SiO_2 interface. Poisson equation is solved by 3-dimentional device simulator.

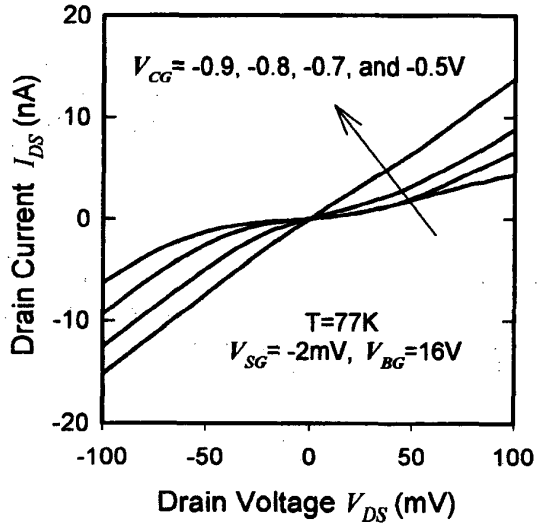

FIG. 5. Drain voltage dependence of the drain current of SET1 at 77 K. Coulomb gap is clear and modulated by V_{CG}.

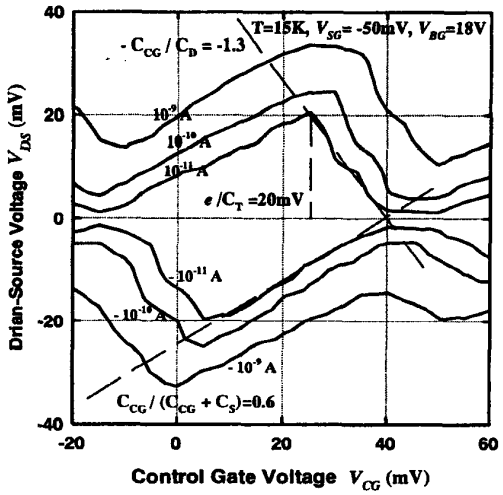

FIG. 6. Contour plot of drain current as a function of control gate voltage (V_{CG}) and drain voltage (V_{DS}) of SET2 at 15 K. The voltage gain of 1.3 is obtained.