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Double-dot-like charge transport through a small size silicon single electron transistor

B.H. Choi[a,b], Y.S. Yu[a,b], D.H. Kim[c], S.H. Son[a], K.H. Cho[a], S.W. Hwang[a,b,*], D. Ahn[b], B.G. Park[c]

[a]*School of Electrical Engineering, Korea University, Anam-dong, Sungbuk-ku, Seoul 136-075, South Korea*
[b]*Institute of Quantum Information Processing and Systems, University of Seoul, Jeonnong-dong, Dongdaemun-ku, Seoul 130-743, South Korea*
[c]*School of Electrical Engineering, Seoul National University, San 56-1, Shinlim-dong, Kwanak-gu, Seoul 151-742, South Korea*

Abstract

We report double dot like charge transport in a Si single electron transistor with a single fabricated dot. Detailed analysis of the transport data suggests the existence of another quantum dot with a size much larger than the fabricated dot. More importantly, it is shown that the Coulomb oscillations observed at high temperature clearly originate from the fabricated dot. Possible origin of the accidental formation of the second quantum dot is either a defect at the Si/buried oxide interface or a defect in the thermal oxide surrounding the Si quantum wire. © 2002 Elsevier Science B.V. All rights reserved.

Keywords: Si quantum dot; Double dot; Transport; Single electron transistor

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Earlier experimental observation of single electron tunneling in semiconductor quantum structures was realized in quantum wires fabricated from a GaAs/AlGaAs heterostructure [1] and a silicon (Si) inversion layer [2]. In both cases, quantum dots that are accidentally formed in narrow channels were responsible for the observed Coulomb oscillations. In the case of GaAs/AlGaAs heterostructures, random dopant distribution was shown to give long-range potential fluctuations [3], and many interesting measurements from intentional series [4] and parallel [5] dot structures have revealed various line shapes of Coulomb oscillations. On the other hand, the origin of potential fluctuations, and therefore, the formation of unintentional tunnel barriers in Si has not been studied intensively. In this paper, we report double dot like charge transport in a Si single electron transistor (SET) with a single fabricated dot. Detailed analysis of the transport data suggests the existence of another quantum dot with a size much larger than the intentionally fabricated dot. More importantly, it is shown that the Coulomb oscillations observed at high temperature (T) clearly originate from the intentionally fabricated dot. Possible origin of the accidental formation of the quantum dot is either defect at a Si/buried oxide interface or a defect in the thermal oxide surrounding the Si quantum wire.

Fig. 1 shows a schematic sketch of the Si SET we have studied. It has been fabricated on a 10^{15} cm^{-3} boron-doped p-type silicon-on-insulator (SOI) wafer. The thickness of the buried oxide is 415 nm and the

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* Corresponding author. School of Electrical Engineering, Korea University, Anam-dong, Sungbuk-ku, Seoul 136-075, South Korea. Tel.: +82-2-3290-3241; fax: +82-2-927-6114.

E-mail address: swhwang@korea.ac.kr (S.W. Hwang).

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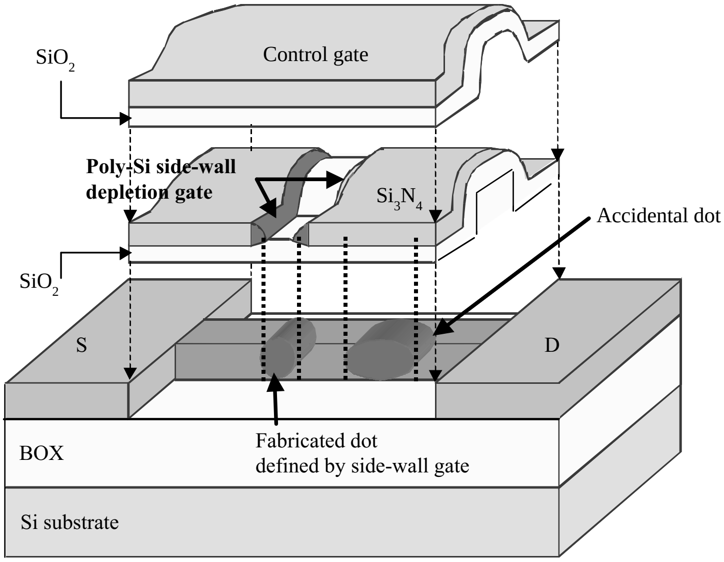

Fig. 1. A schematic sketch of the fabricated Si SET. The intentionally fabricated quantum dot is formed by the two Poly-Si side-wall depletion gates. The accidental quantum dot may be located in the thermal oxide surrounding the Si quantum wire. Other possibility is that unintentional defects create accidental dot near the fabricated dot.

top Si layer has been thinned down to 30 nm. A quantum wire with the width of 30 nm has been formed using side-wall definition technique by conventional photo-lithography [6], so that the fluctuation of the wire width is suppressed within 2 nm. Quantum wires defined by electron beam lithography showed much larger fluctuations in the wire width [7]. Two side gates with the separation of 37 nm have been made on the wire for the definition of the quantum dot. Subsequently, a thick layer of SiO_2 and a poly-silicon control gate have been formed. The inversion layer in the Si channel was formed by the back gate bias, and the total charge of the quantum dot was controlled by the control gate. Detailed process sequences have been reported elsewhere [8].

Fig. 2 shows the drain current-control gate voltage (I_{DS}–V_{CG}) characteristics measured at $T = 4.2$ K. Coulomb blockade oscillation peaks with the periodicity of 24 mV are strongly modulated with a larger periodicity of 430 mV. Such modulation is a strong evidence for the double-dot transport [8]. The gate capacitance (C_{G1}) of a smaller dot (dot 1) extracted from the longer periodicity is 0.377 aF. The gate capacitance (C_{G2}) of a larger dot (dot 2) obtained from the shorter periodicity is 6.78 aF. Fig. 2(b) shows the I_{DS}–V_{CG} characteristics measured at $T = 85$ K from a similar sample with the same spacing between two side gates. It shows Coulomb oscillations of the periodicity of 440 mV that is similar to the longer period of the first sample. This suggests that the longer period oscillations of Fig. 2(a) are originated from the quantum dot defined by the side gates. Moreover, from Fig. 2(b), it is shown that the Coulomb oscillations observed at high T are clearly originated from the fabricated dot.

The modulated conductance oscillations in Fig. 2 has been analyzed by the model of two dots in series. The KOSEC (KOrea Single Electron Circuit simulator) [9] has been used to calculate the current as a function of the control gate bias from the equivalent circuit of Fig. 3. The gate capacitance values of C_{G1} and C_{G2} are fixed at the values obtained from the data of Fig. 2 (0.377 and 6.78 aF, respectively). The drain capacitance (C_D) and the source capacitance (C_S) extracted from V_{CG}–V_{DS} contour plot (not shown here) are 2.37 and 5.37 aF, respectively. The value of the coupling capacitance (C_C) is optimized against the measured data, and $C_C = 1.0$ aF gives the best fit with the measured data. Fig. 4(a) shows the simulation result using the above parameters. All the qualitative features of

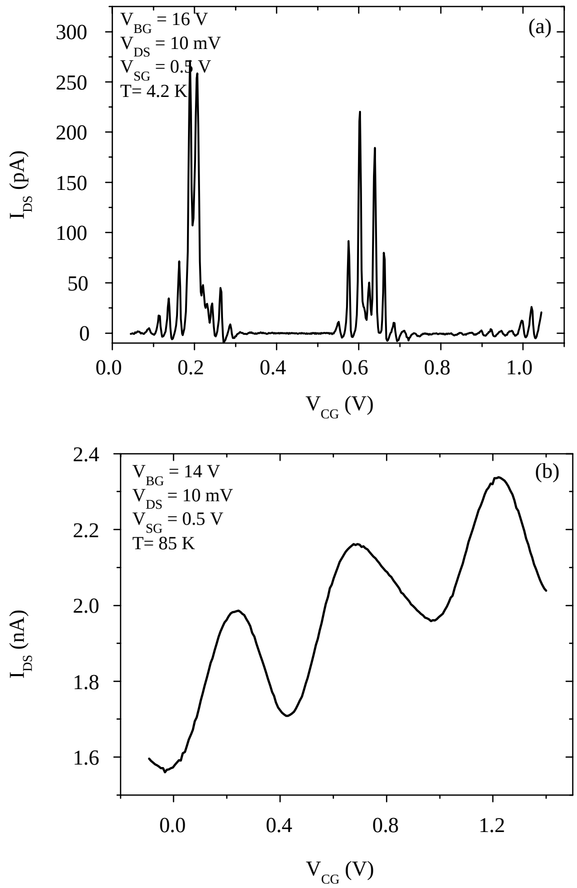

Fig. 2. (a) The I_{DS}–V_{CG} characteristics measured at 4.2 K. Coulomb blockade oscillations with small periodicity are strongly modulated with longer periodicity. (b) The I_{DS}–V_{CG} characteristics measured at 85 K from another sample from the same batch. At this high temperature, unlike the characteristics at the $T = 4.2$ K, only Coulomb oscillations with longer periodicity were observed.

the measured data are clearly reproduced. The shape of the modulation is a strong function of C_C. Fig. 4(b) shows the calculated I_{DS}–V_{CG} characteristics at various C_C values from 0.1 to 10 aF. The simulation of the Fig. 4(b) is performed with the value of the tunneling rates that are adjusted by the maximum I_{DS} in the I_{DS} oscillation. The relative decrease of I_{DS} from the maximum value is a strong function of C_C.

The charging energy obtained from the total capacitance of the dot 1 ($C_{G1} + C_D + C_C = 3.8$ aF) is 21.4 meV. It is consistent with the geometrical size of the intentionally fabricated quantum dot. On the

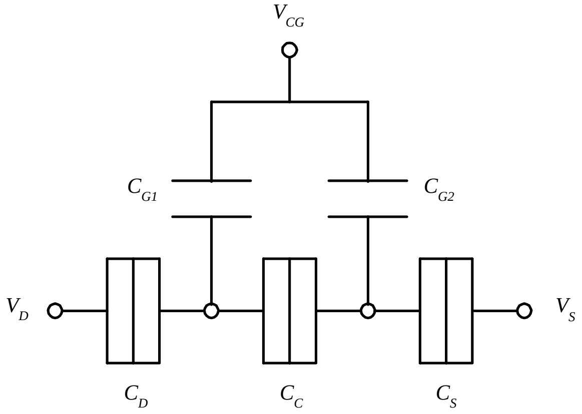

Fig. 3. The equivalent circuit used in the simulation.

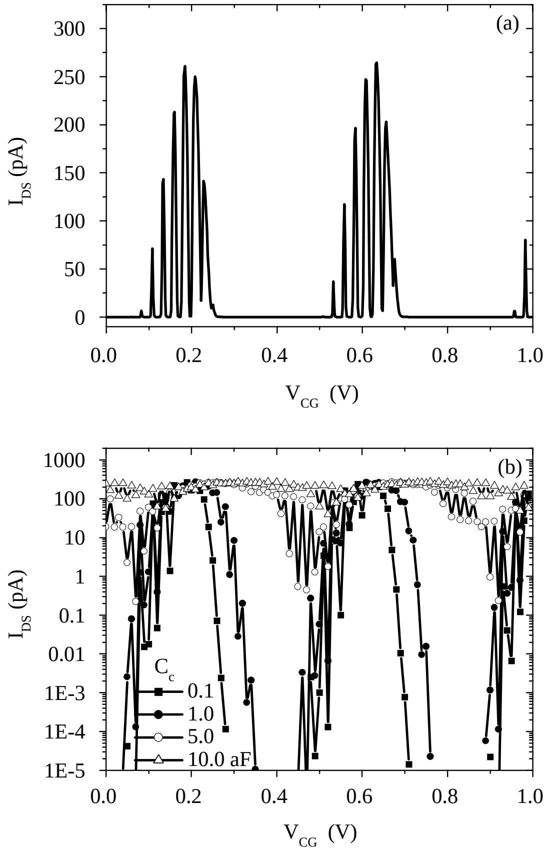

Fig. 4. The simulation result of I_{DS}–V_{CG} characteristics assuming $C_C = 1.0$ aF. $C_C = 1.0$ aF gives the best fit with the measured result. (b) The simulation result of I_{DS}–V_{CG} at various C_C values in log scale. ((■) denotes $C_C = 0.1$, (●) 1.0, (○) 5.0 and (△) 10.0 aF, respectively.).

other hand, the charging energy of the dot 2 (C_T of dot 2: $C_{G2} + C_S + C_C = 13.2$ aF) is estimated to be 6.1 meV, which is 3.5 times smaller than that of the dot 1. This value corresponds to a quantum dot with the radius of 61 nm. The total length of the fabricated quantum wire is 5 μm and the defect density at the top Si and the buried oxide interface is 1–2/cm^2. There is only a little possibility that unintentional defects create another quantum dot near the fabricated quantum dot. The other possibility is that an accidental defect in thermal oxide surrounding the quantum wire creates a barrier [10].

In summary, we report double dot like charge transport in Si SET with a single intentionally fabricated dot. Detailed analysis of the transport data suggests the existence of another quantum dot with a size much larger than the fabricated dot. More importantly, it is shown that the Coulomb oscillations observed at high temperature clearly originate from the fabricated dot. Possible origin of the accidental formation of the quantum dot is either a defect at the Si/buried oxide interface or a defect in the thermal oxide surrounding the Si quantum wire.

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