Single-Electron Transistors Based on Gate-Induced Si Island for Single-Electron Logic Application

Dae Hwan Kim, Suk-Kang Sung, Kyung Rok Kim, Jong Duk Lee, *Member, IEEE*, and Byung-Gook Park, *Member, IEEE*

***Abstract*—The island size dependence of the capacitance components of single-electron transistors (SETs) based on gate-induced Si islands was extracted from the electrical characteristics. In the fabricated SETs, the sidewall gate tunes the electrically induced tunnel junctions, and controls the phase of the Coulomb oscillation. The capacitance between the sidewall gate and the Si island extracted from the Coulomb oscillation phase shift of the SETs with sidewall depletion gates on a silicon-on-insulator nanowire was independent of the Si island size, which is consistent with the device structure. The Coulomb oscillation phase shift of the fabricated SETs has the potential for a complementary operation. As a possible application to single-electron logic, the complementary single-electron inverter and binary decision diagram operation on the basis of the Coulomb oscillation phase shift and the tunable tunnel junctions were demonstrated.**

***Index Terms*—Binary decision diagram, gate-induced island, sidewall gate, single-electron inverter, SOI.**

I. Introduction

SI-BASED single-electron transistors (SETs) have been widely studied and demonstrated due to the maturity and variety of their process technologies. Devices based on the single-electron charging effect, i.e., the Coulomb blockade in Si nanostructures, are promising because their operation principle becomes more robust as the device size is scaled down. Moreover, their power consumption is quite low. However, SETs are not expected to replace the conventional CMOS logic devices because of their inherent limitations such as a low voltage gain and current drivability. In contrast, new functionalities of SETs, such as quantum cellular automata (QCA) [1], [2], binary decision diagram (BDD) devices [3], [4], and the multivalued logic [5], have been explored extensively. In order to investigate and optimize the new circuit architecture, a reproducible structure of Si-based SETs featuring tunable tunnel junctions and a complementary operation as in CMOS devices are required. Compared to SETs based on either lithographically defined Si islands [6] or accidentally formed Si islands [7], [8], the SETs based on gate-induced Si islands are more promising in terms of their strong confinement and reproducibility.

Manuscript received June 7, 2002; revised October 23, 2002. Revised for the publication in special issue on collaboration with the Si Nanoelectronics Workshop 2002. This work was supported by the BK 21 Program, by the Ministry of Commerce, Industry and Energy under the "Functional Nano-Device & Circuit Application Technology Development Project," and by the National Program for the "Tera-bit Level Nano Device Project" as a part of 21st Century Frontier Project.

The authors are with the Inter-University Semiconductor Research Center (ISRC) and School of Electrical Engineering, Seoul National University, Seoul 151-742, Korea (e-mail: drlife@smdl.snu.ac.kr; bgpark@snu.ac.kr)

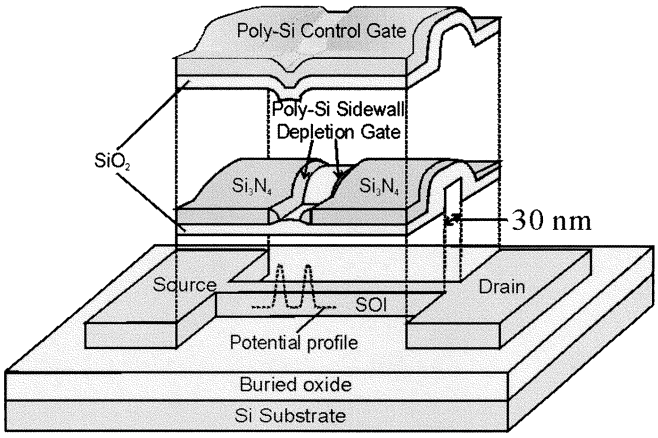
Digital Object Identifier 10.1109/TNANO.2002.807382

On the other hand, the compatibility with conventional Si technology is another challenge for evaluating the functionality of a MOSFET-SET hybrid circuit. Among various approaches for SETs based on gate-induced Si islands [9]–[12], the SETs with sidewall depletion gates on a silicon-on-insulator (SOI) nanowire reported in this study showed that the device parameters such as the control gate capacitance and the tunnel junction capacitance, as well as a relatively high operation temperature, were reproducible [13]. Moreover, their dynamic multifunctional logic operation has already been demonstrated. In the proposed logic scheme, the capacitance between the sidewall gate and the Si island is another critical parameter, which should be further investigated, because the sidewall gate voltage is used as an input signal [14].

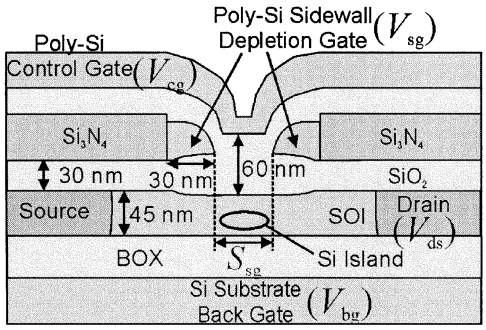
In this paper, the capacitance between the sidewall gate and the Si island was extracted from the Coulomb oscillation phase shift by modulating the sidewall gate voltage, and its island size dependence was studied. It was found that the sidewall gate capacitance is independent of the size of the Si island, which is consistent with the device structure. In addition, the complementary single-electron inverter and the BDD operation were demonstrated on the basis of the Coulomb oscillation phase shift and the tunable tunnel junctions. The former is an application conceptually similar to our previous work [14], where the sidewall gate voltage was reported to control only a single-electron tunneling condition. However, the latter is another promising application, which is suitable for the gate-induced Si island. This is because the two functions of the sidewall gate i.e., not only inducing a tunnel barrier but also squeezing the conducting channel, were used effectively.

II. Device Structure and Electrical Characteristics

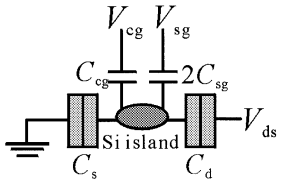
The device was fabricated on 4×10^{15} cm^{-3} boron-doped (100) SOI wafers prepared by the separation by implanted oxygen (SIMOX) technique. Fig. 1 shows the schematic and equivalent circuit diagram of the SET with sidewall depletion gates on a SOI nanowire. The width and height of the SOI wire were 30 and 45 nm, respectively. This wire was defined by means of the sidewall patterning method. The very uniform weakly p-doped SOI nanowires defined by this patterning method have already been reported to effectively suppress unintentional tunnel junctions formed by fluctuations in the geometry or the impurity potential in the SOI wire, and the gate-induced Si island size dependence of the device characteristics confirmed the good controllability [14]. The device operation is as follows: The electron channel in the SOI wire is formed by the back gate voltage $V_{\rm bg}$, and two tunnel



(a)



(b)



(c)

Fig. 1. (a) Schematic diagram of the SET with sidewall depletion gates on a SOI nanowire. (b) Cross-section of the fabricated SET. (Reprinted from [14]). (c) Equivalent circuit diagram of the fabricated SET. Because of the relatively thick buried oxide, the capacitance between the backgate and the Si island is neglected.

junctions are formed by the sidewall depletion gate voltage $V_{\rm sg}$. The electrostatic potential of the gate-induced Si island is controlled by the control gate voltage $V_{\rm cg}$. The effective size of the gate-induced Si island is controlled from 40 to 190 nm by varying the separation between the two sidewall depletion gates $S_{\rm sg}$, while the thickness of the control gate oxide is fixed to 60 nm. Details of the fabrication method are reported elsewhere [14]. The main feature of the fabrication method is that all critical dimensions depend not on the limit of lithography but on the controllability of the conventional Si technology.

Fig. 2 shows the temperature dependence of the drain current $I_{\rm ds}$-$V_{\rm cg}$ characteristics of the SETs with $S_{\rm sg} = 40$ nm, which suggests reliable single-island characteristics. The Coulomb oscillation can be observed clearly even up to 188 K. The total capacitance of the gate-induced Si island $C_{\rm total}$ was estimated to be approximately 2.86 aF, which is consistent with the operation temperature. In these devices, the island size $S_{\rm sg}$, dependence of both the capacitance between the control gate and island $C_{\rm cg}$, and the capacitance of the drain tunnel junction $C_{\rm d}$,

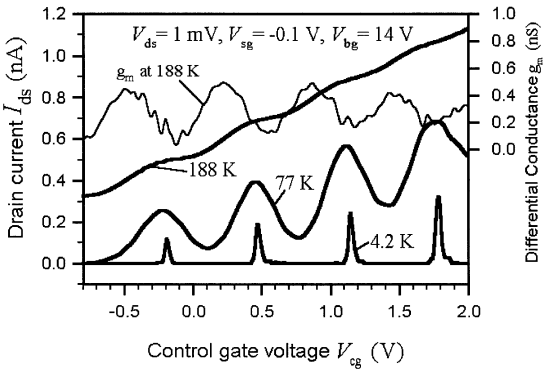


Fig. 2. Temperature dependence of the Coulomb oscillation characteristics of the SET with $S_{\rm sg} = 40$ nm.

were systematically studied [14]. The result confirms that the measured current–voltage (I-V) characteristics originated from the designed gate-induced Si island embedded in the electron channel of the SOI MOSFETs. In contrast, the $V_{\rm cg}$ value, where the energy degeneracy between the two states of the electron numbers in the Si island occurs, can be modulated by varying the $V_{\rm sg}$ because of capacitive coupling between the $C_{\rm cg}$ and the capacitance between the sidewall gate and island $C_{\rm sg}$. This can be observed as the Coulomb oscillation phase shift by the $V_{\rm sg}$ modulation, as shown in Fig. 3. The $C_{\rm sg}$ can be extracted from the measured shift of the Coulomb oscillation phase in Fig. 3. Based on the conservation of island charge, the relationship between the shift of the oscillation peak in the $V_{\rm cg}$ axis ($\Delta V_{\rm cg}$) and the change of $V_{\rm sg}$ ($\Delta V_{\rm sg}$) is derived as follows:

$$\Delta V_{\rm cg} = -\frac{2C_{\rm sg}}{C_{\rm cg}} \times \Delta V_{\rm sg} \tag{1}$$

where a factor of two indicates that the $C_{\rm sg}$ is the capacitance between a single sidewall gate and the island and the minus sign reflects the fact that the peak position shifts to the left direction as the $V_{\rm sg}$ increases.

From these results, the island size dependence of the capacitance components of the fabricated SETs can be summarized as shown in Fig. 4. Both $C_{\rm cg}$ and $C_{\rm d}$ were obtained from the same data in our previous work [14], where the data was taken from seven different SETs with the same $S_{\rm sg}$ and the error bar shows the standard deviation of 21 experiments (setting $V_{\rm sg}$ to be 0, -0.05, and -0.1 V in each SET). While the $C_{\rm cg}$ has a linear relationship with the $S_{\rm sg}$, the $S_{\rm sg}$ dependence of $C_{\rm d}$ is less prominent and the $C_{\rm sg}$ is independent of $S_{\rm sg}$. This result is consistent with the device structure, because the sidewall gate structure is the same while the $S_{\rm sg}$ varies. Therefore, the device parameters can be controlled by the device structure.

III. Complementary Single-Electron Inverter and BDD Devices

In the SETs in this study, the Coulomb oscillation phase shift can be controlled by the $V_{\rm sg}$, without an additional gate, which originates from island charge sharing between the control gate and the sidewall depletion gates. Therefore, the usage of the $V_{\rm sg}$ as the digital input compensates for the loss in the integration density and makes the complementary logic or the multi-gate

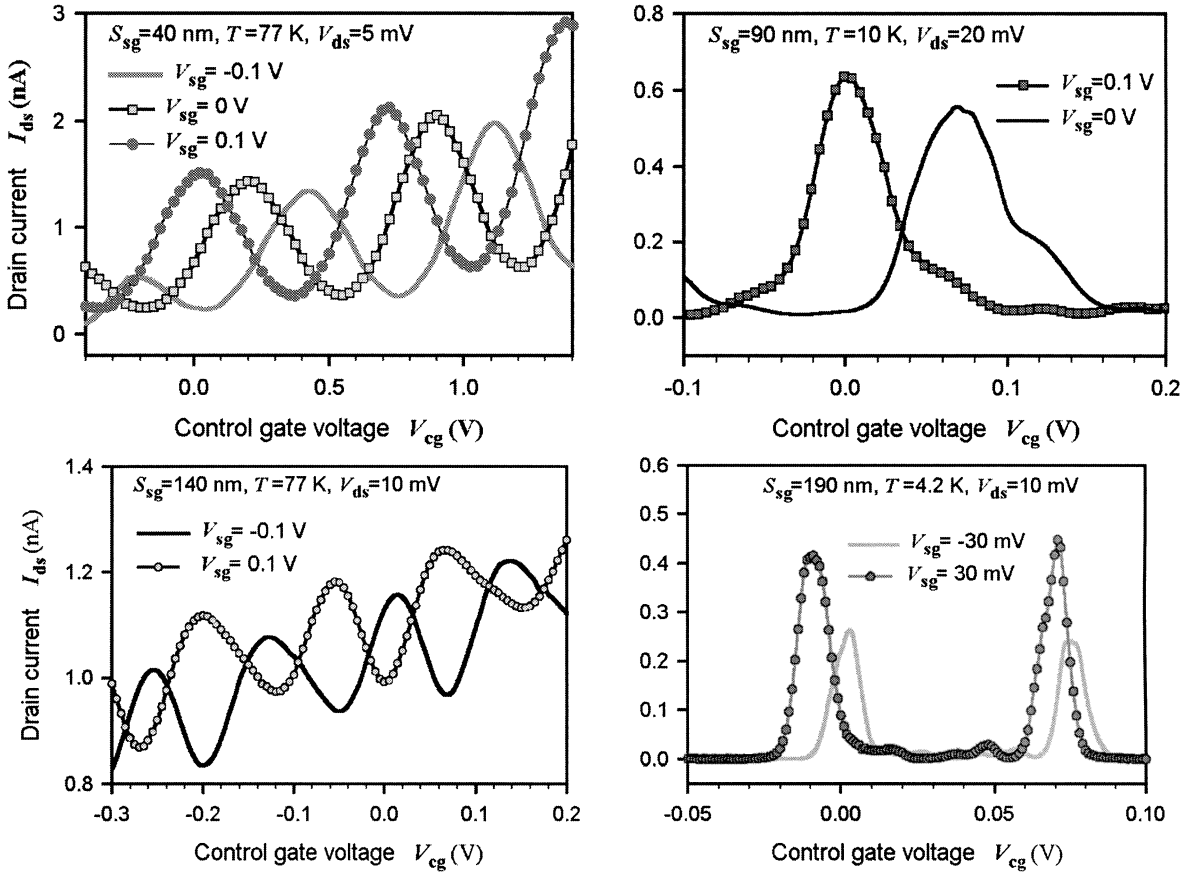


Fig. 3. The $V_{\rm sg}$ dependences of the Coulomb oscillations of the SETs with various $S_{\rm sg}$'s. The $C_{\rm sg}$ was estimated to be 0.24, 0.27, 0.23 and 0.22 aF, respectively, as the $S_{\rm sg}$ is varied from 40 to 190 nm.

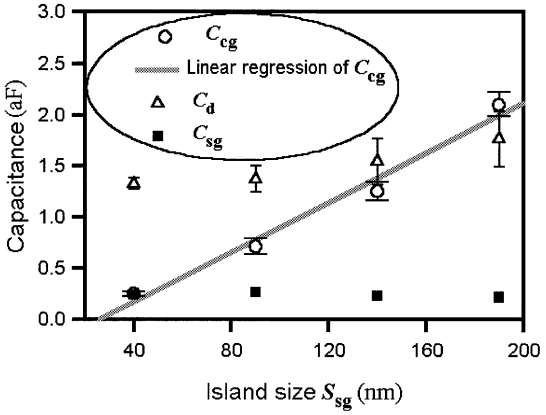


Fig. 4. Island size dependence of the capacitance components of the fabricated SETs.

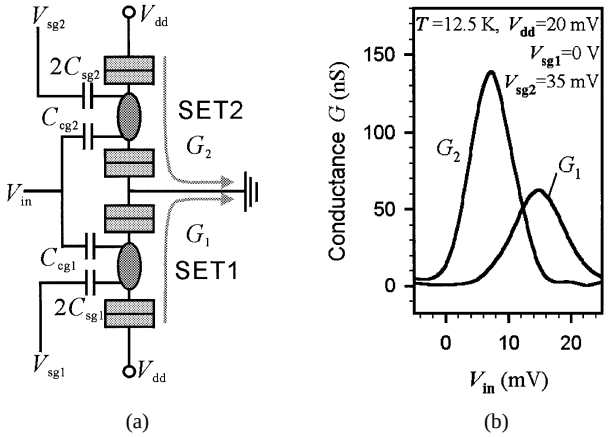


Fig. 5. (a) Circuit diagram of the directional current switch and (b) its conductance characteristic at 12.5 K. This conductance was measured, while the $V_{\rm ds}$, $V_{\rm sg1}$ and $V_{\rm sg2}$ were fixed at 20 mV, 0 V, and 35 mV, respectively.

logic possible [15], [16]. Furthermore, when a negatively large $V_{\rm sg}$ is applied, the tunneling of a single electron is fully blocked due to a very high potential barrier.

The complementary operation of our SETs can be applied to a CMOS-like single-electron inverter [17]. Fig. 5(a) shows the directional current switch implemented by two SETs with a $S_{\rm sg}$ of 190 nm. By tuning the respective $V_{\rm sg}$ of the two SETs, the conductance G through each SET is complementarily switched, as shown in Fig. 5(b). This conductance was measured at 12.5 K, while the $V_{\rm ds}$, $V_{\rm sg1}$, and $V_{\rm sg2}$ were fixed at 20 mV, 0 V, and 35 mV, respectively. Based on the complementary conductance characteristics, a single-electron inverter was implemented as shown in Fig. 6(a). Fig. 6(b) shows its voltage transfer characteristic at a supply voltage $V_{\rm dd}$ of 20 mV and a temperature of 12.5 K. The inverter characteristic with a voltage gain of approximately 1.4 was successfully demonstrated. Although this complementary operation is useful, the CMOS-like SET logic is not so promising, as described in the Introduction.

On the other hand, the concept of BDD devices [3], [18] is more promising for a new single-electron logic circuit, because the drawback of a low current drivability and voltage gain is

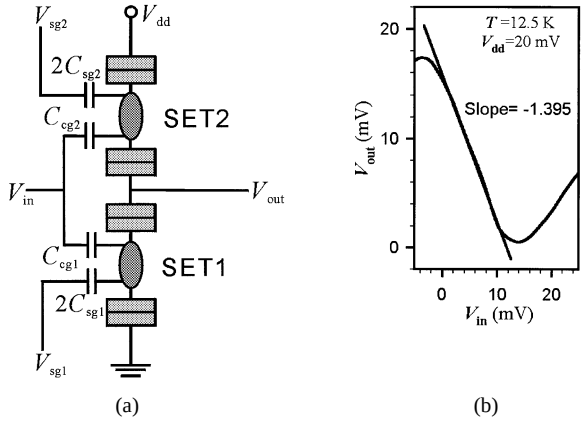


Fig. 6. (a) Circuit diagram of the complementary single-electron inverter and (b) its voltage transfer characteristics at 12.5 K. The $V_{\rm ds}$, $V_{\rm sg1}$ and $V_{\rm sg2}$ were fixed at 20 mV, 0 V, and 35 mV, respectively.

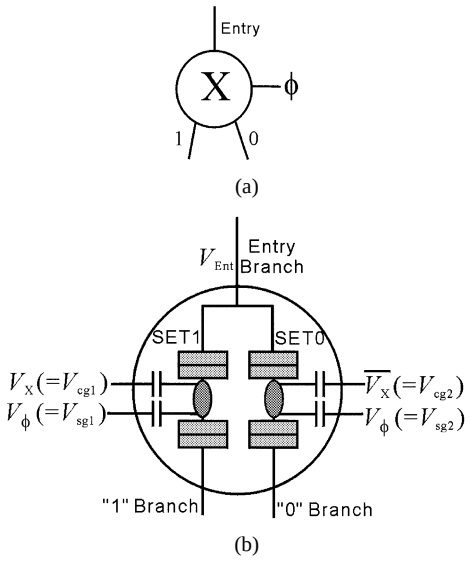


Fig. 7. (a) The symbol and (b) circuit diagram of the unit device for the single-electron BDD logic circuit.

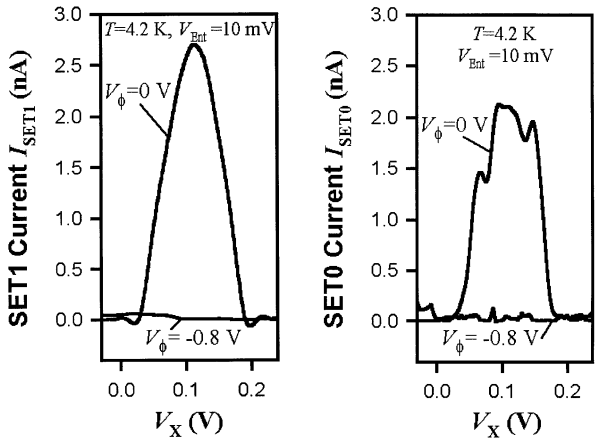


Fig. 8. The clock signal V_ϕ-dependence of the SET current of (a) "1" branch and (b) "0" branch at 4.2 K.

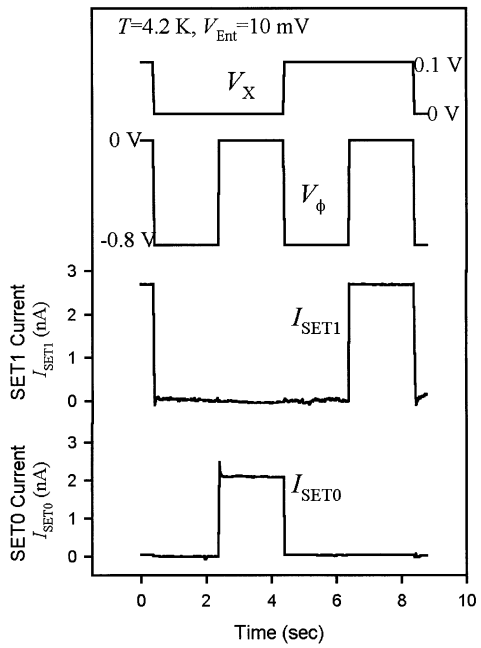


Fig. 9. Experimental demonstration of single-electron BDD logic circuit at 4.2 K. The input voltage V_X was applied synchronously with the clock signal, V_ϕ. When $V_\phi = -0.8$ V, single-electron tunneling is fully blocked due to the high potential barrier.

less conspicuous. Using a single-electron BDD structure, one can implement the general Boolean functions. Fig. 7 shows a symbol and the circuit diagram of the unit device for a BDD logic circuit implemented by two fabricated SETs. In order to eliminate the error by unwanted tunneling events, the transfer of a single electron in the other unit devices should be synchronously blocked when the input voltage, V_X, was applied to a one unit device synchronously with the clock signal, V_ϕ. This requirement can be satisfied in our devices by applying a negatively large V_ϕ to the sidewall depletion gates, without an additional pass gate for the clock signal. Fig. 8(a) and 8(b) show the V_ϕ dependence of the two SETs currents used in implementing the unit device of the single-electron BDD system. Their $S_{\rm sg}$'s are both 90 nm and the $SETi$ is a symbol for the device for the i branch. Their currents (I_{SET0} and I_{SET1}) were measured at 4.2 K by fixing the drain voltage i.e., $V_{\rm Ent}$ to 10 mV and the source voltage to the ground. When V_ϕ is -0.8 V, the transfer of a single electron is fully blocked. Fig. 9 shows that only when V_ϕ is 0 V can a single electron transfer through a corresponding branch, which is the core operation of the BDD devices.

While the BDD structure proposed by Asahi *et al.*. was based on the electron-transfer circuit known as a single-electron pump [3], the BDD unit device shown in Fig. 7(b) uses the SETs as switches. In a single-electron pump, only a single electron is used as a messenger. Therefore, the amplitude of the output signal is determined only by the clock frequency. However, in this study, the amplitude of the output signal is determined by both the clock frequency and the bias condition and a few electrons are tranferred in one clock cycle. Although a single-electron pump has the merit of ultra-low power consumption, it is very difficult to implement. On the other hand, the concept of a BDD operation based on electrically depleting the conduction channel has been already demonstrated in a gated narrow wire defined in the δ-doped GaAs channel [19], where the devices were biased on two conditions; a pinch-off and the lift of

a Coulomb blockade. However, in this study, the SETs were biased on three operational conditions; a pinch-off, the "ON" state of a SET and the "OFF" state of a SET. The scheme of processing the inputs and a clock signal can be diversely optimized with a correspondence to the various implementation methods of the BDD logic circuit. For a quantitative comparison, an extensive simulation study is strongly recommended.

IV. Conclusion

The island size dependence of the capacitance components of SETs based on the gate-induced Si island is discussed. The capacitance between the sidewall gate and the Si island extracted from the Coulomb oscillation phase shift of the SETs with sidewall depletion gates on a SOI nanowire was found to be independent of the island size, which is consistent with the device structure. As a possible application of the oscillation phase shift by the sidewall depletion gates, the operation of the complementary single-electron inverter was demonstrated at 12.5 K. Furthermore, the operation of the unit device for a single-electron BDD circuit was demonstrated at 4.2 K, on the basis of the Coulomb oscillation phase shift and the tunable tunnel junctions. The structure of the fabricated SETs will be very useful for device design and optimization in order to explore a new functional SET circuit architecture.

References

[1] C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernstein, "Quantum cellular automata," *Nanotechnology*, vol. 4, pp. 49–57, 1993.

[2] C. S. Lent and P. D. Tougaw, "A device architecture for computing with quantum dots," *Proc. IEEE*, vol. 85, pp. 541–557, 1997.

[3] N. Asahi, M. Akazawa, and Y. Amemiya, "Single-electron logic device based on the binary decision diagram," *IEEE Trans. Electron Devices*, vol. 44, pp. 1109–1116, 1997.

[4] S. Kasai, Y. Amemiya, and H. Hasegawa, "GaAs Schottky wrap-gate binary-decision-diagram devices for realization of novel single electron logic architecture," in *IEDM Tech. Dig.*, 2000, pp. 585–588.

[5] H. Inokawa, A. Fujiwara, and Y. Takahashi, "A multiple-valued logic with merged single-electron and MOS transistors," in *IEDM Tech. Dig.*, 2001, pp. 147–150.

[6] L. Zhuang, L. Guo, and S. Y. Chou, "Silicon single-electron quantum-dot transistor switch operating at room temperature," *Appl. Phys. Lett.*, vol. 72, no. 10, pp. 1205–1207, 1998.

[7] H. Ishikuro and T. Hiramoto, "Quantum mechanical effects in the silicon quantum dot in a single-electron transistor," *Appl. Phys. Lett.*, vol. 71, no. 25, pp. 3691–3693, 1997.

[8] A. C. Irvine, Z. A. K. Durani, H. Ahmed, and S. Biesemans, "Single-electron effects in heavily doped polycrystalline silicon nanowires," *Appl. Phys. Lett.*, vol. 73, no. 8, pp. 1113–1115, 1998.

[9] H. Matsuoka and S. Kimura, "Transport properties of a silicon single-electron transistor at 4.2 K," *Appl. Phys. Lett.*, vol. 66, no. 5, pp. 613–615, 1995.

[10] M. Khoury, M. J. Rack, A. Gunther, and D. K. Ferry, "Spectroscopy of a silicon quantum dot," *Appl. Phys. Lett.*, vol. 74, no. 11, pp. 1576–1578, 1999.

[11] F. Simmel, D. Abusch-Magder, D. A. Wharam, M. A. Kastner, and J. P. Kotthaus, "Statistics of the Coulomb-blockade peak spacings of a silicon quantum dot," *Phys. Rev. B*, vol. 59, no. 16, pp. R10441–R10444, 1999.

[12] D. H. Kim, J. D. Lee, and B.-G. Park, "Room temperature Coulomb oscillation of a single electron switch with an electrically formed quantum dot and its modeling," *Jpn. J. Appl. Phys.*, vol. 39, no. 4B, pp. 2329–2333, 2000.

[13] D. H. Kim, S.-K. Sung, K. R. Kim, B. H. Choi, S. W. Hwang, D. Ahn, J. D. Lee, and B.-G. Park, "Si single-electron transistors with sidewall depletion gates and their application to dynamic single-electron transistor logic," in *IEDM Tech. Dig.*, 2001, pp. 151–154.

[14] D. H. Kim, S.-K. Sung, K. R. Kim, J. D. Lee, B.-G. Park, B. H. Choi, S. W. Hwang, and D. Ahn, "Silicon single-electron transistors with sidewall depletion gates and their application to dynamic single-electron transistor logic," *IEEE Trans. Electron Devices*, vol. 49, pp. 627–635, 2002.

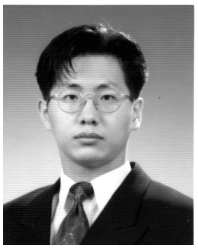
[15] Y. Takahashi, A. Fujiwara, K. Yamazaki, H. Namatsu, K. Kurihara, and K. Murase, "A multi-gate single-electron transistor and its application to an exclusive-OR gate," in *IEDM Tech. Dig.*, 1998, pp. 127–130.

[16] Y. Ono and Y. Takahashi, "Single-electron pass-transistor logic and its application to a binary adder," in *Proc. Symp. VLSI Circuits*, 2001, pp. 63–66.

[17] Y. Ono, Y. Takahashi, K. Yamazaki, M. Nagase, H. Namatsu, K. Kurihara, and K. Murase, "Si complementary single-electron inverter," in *IEDM Tech. Dig.*, 1999, pp. 367–370.

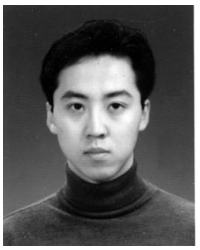
[18] N. Asahi, M. Akazawa, and Y. Amemiya, "Binary-decision-diagram device," *IEEE Trans. Electron Devices*, vol. 42, pp. 1999–2003, 1995.

[19] K. Tsukagoshi, B. W. Alphenaar, and K. Nakazato, "Operation of logic function in a Coulomb blockade device," *Appl. Phys. Lett.*, vol. 73, no. 17, pp. 2515–2517, 1998.



Dae Hwan Kim was born in Seoul, Korea in 1972. He received the B.S., M.S., and Ph.D. degrees from the School of Electrical Engineering, Seoul National University, Seoul, Korea, in 1996, 1998, and 2002, respectively.

He joined Samsung Electronics Corporation, Kyungki-Do, Korea, in 2002, where he has been engaged in circuit design of DRAM. His current research interests are Si nanoelectronic devices and nanoscale CMOS devices.



Suk-Kang Sung was born in Korea, in 1973. He received the B.S. and M.S. degrees from School of Electrical Engineering, Seoul National University, Seoul, Korea, in 1997 and 1999, respectively. Since 1999, he has been pursuing the Ph.D. degree at the same university. His current research interests are Si nanoelectronic devices and single-electron memory.

Kyung Rok Kim received the B.S. and M.S. degrees in 1999 and 2001, respectively, from the School of Electrical Engineering, Seoul National University, Seoul, Korea, where he is currently working toward the Ph.D. degree.

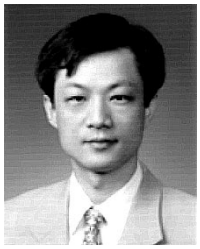
His current research interest is Si quantum tunneling device.

Jong Duk Lee (M'79) was born in Kyungpook, Korea, in 1944. He received the B.S. degree in physics from Seoul National University, Seoul, Korea, in 1966, and the Ph.D. degree from the Department of Physics, University of North Carolina, Chapel Hill, in 1975.

He was an Assistant Professor in the Department of Electronics Engineering, Kyungpook National University, Kyungpook, Korea, from 1975 to 1978. In 1978, he studied microelectric technology at HP-ICL, Palo Alto, CA and soon afterward, joined the Korea Institute of Electronic Technology (KIET) as the Director of the Semiconductor Division, Daegu. He established the KIET Kumi Facility and introduced the

first polysilicon gate technology in Korea by developing 4K SRAM, 32K and 64K Mask ROMs, and one-chip 8-bit microcomputers. In July 1983, he moved to the Department of Electronics Engineering, Seoul National University, as an Associate Professor, which merged with the School of Electrical Engineering in 1992, where he has been aProfessor since 1988. He established the Inter-University Semiconductor Research Center (ISRC) in 1985 and served as the Director until 1989. He served as the Chairman of the Electronics Engineering Department from 1994 to 1996. During 1996, he was on leave with Samsung Display Devices Co., Ltd., Suwon, Korea, as the Head of Display R&D Center. During 1984 to 1991, he studied image sensors types such as Vidicon, MOS, and CCDs, for Samsung Display Devices Co. and Samsung Electronics Company. His current research interests include sub-0.1 μm CMOS structure and technology, FEDs, CMOS image sensor and high-speed SRAM design. He has published over 130 papers in major international scientific journals, including over 65 SCI papers. He has presented more than 180 papers, including 80 international conference papers. He also has 11 U.S., 3 Japanese, and 8 Korean registered patents.

Dr. Lee is a member of the Steering Committee for the International Vacuum Microelectronics Conference (IVMC) and Korean Conference on Semiconductors (KCS), and was previously a member of the International Electron Devices Meeting (IEDM) Subcommittee on Detectors, Sensors and Displays operated by IEEE Electron Devices Society from 1998 to 1999. He was the Conference Chairman of IVMC'97 and KCS'98. In June 1999, he was elected First President of the Korean Information Display Society.



Byung-Gook Park (M'90) received the B.S. and M.S. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1982 and 1984, respectively and his Ph.D. degree in Electrical Engineering from Stanford University, Stanford, CA, in 1990.

From 1990 to 1993, he worked at the AT&T Bell Laboratories, Murray Hill, NJ, where he contributed to the development of 0.1-μm CMOS and its characterization. From 1993 to 1994, he was with Texas Instruments, Dallas, TX, developing 0.25-μm CMOS. In 1994, he joined the School of Electrical Engineering, Seoul National University, as an Assistant Professor; and he is currently an Associate Professor. He has been a member of IEDM (International Electron Devices Meeting) Subcommittee on Solid State Devices, operated by IEEE Electron Devices Society from 2001 to 2002. His current research interests are nanoscale CMOS devices, Si single-electron devices, organic electroluminescent display and scanning probe microscopy system.