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A SPICE Model of Realistic Single-Electron Transistors and Its Application to Multiple-Valued Logic

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A SPICE (simulation program with integrated circuit emphasis) model for a single-electron transistor (SET) was developed based on the physical phenomena in realistic Si SETs and was implemented into a conventional circuit simulator. In the proposed model, the SET current calculated using an analytic model is combined with the parasitic MOSFET (metal-oxide semiconductor field effect transistor) characteristics, which have been observed in many recently reported SETs formed on Si nanostructures. An extensive comparison leads to good agreement with a reasonable level of accuracy, whre divergent physical phenomena, such as the parasitic MOSFET, the Coulomb oscillation phase shift, and the tunneling resistance modulated by the gate bias, are considered. Employing the SET SPICE model, we confirmed the feasibility of CMOS (complementary metal-oxide semiconductor)/SET hybrid multiple-valued logics (MVLs). A periodic binary converter with a proposed complementary self-biasing scheme showed improved characteristics in terms of stability and performance.

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I. INTRODUCTION

From the viewpoint of the new functionality of single-electron transistors (SETs), such as the CMOS (complementary metal-oxide semiconductor)/SET hybrid circuit systems, the development of a simulation scheme using a conventional circuit simulator is an emerging challenge. Macro-models [1] and analytical SET models [2] for conventional SPICE (simulation program with integrated circuit emphasis) simulators have recently been proposed and successfully verified in terms of their usefulness and accuracy. Nevertheless, these models are unsatisfactory for analyzing and optimizing the performance of SETs in a real chip because they are validated by a comparison with the Monte Carlo simulation results [3] rather than actual experimental data.

In this study, a practical SPICE model based on the physical phenomena in realistic Si SETs was developed and implemented into a conventional SPICE circuit simulator. The SET SPICE model was applied to the simulation of CMOS/SET hybrid multi-valued logic (MVL) circuits in order to evaluate their stability and performance.

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II. SPICE MODEL OF REALISTIC SINGLE-ELECTRON TRANSISTORS

Figure 1(a) shows a schematic diagram of the device structure and the cross-section of a SET with sidewall depletion gates on a SOI (silicon on insulator) nano-wire [4]. An electrically induced Coulomb island is formed in the 30-nm-wide channel (W_{ch}) of the SOI MOSFET (metal-oxide semiconductor field effect transistor) by the field effect of the sidewall depletion gate bias. Figure 1(b) shows the equivalent circuit diagram of the fabricated device, which is composed of an SET and three parasitic MOSFETs; *i.e.*, one MOSFET is parallel to the SET and the other two are in series with the SET. While the two serial parasitic MOSFETs have a long channel length (L = 3.5 um) from the source (or drain) to the island in Fig. 1(a), the parallel MOSFET has a short channel length (L = island size + 2 × (sidewall depletion gate width)).

Figure 2 shows the electrical characteristic of the fabricated SETs. While the Coulomb oscillation is seen with a sweeping control gate voltage (V_{cg}), three physical phenomena, wich are distinguished from the orthodox the-

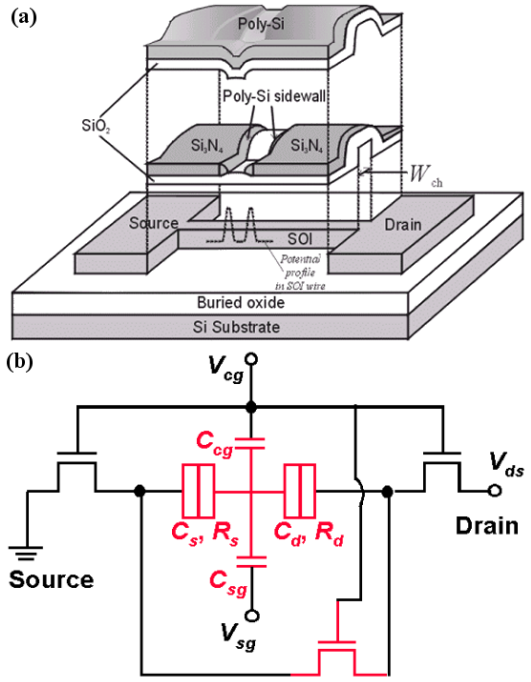

Fig. 1. (a) Schematic diagram of a fabricated Si SET with sidewall depletion gates and (b) equivalent circuit model of (a). Here, the island size S_{sg} can be controlled over the range 40-190 nm. The series and the parallel MOSFETs are used for modeling of the turn-off characteristics and the parallel MOSFET operation, respectively.

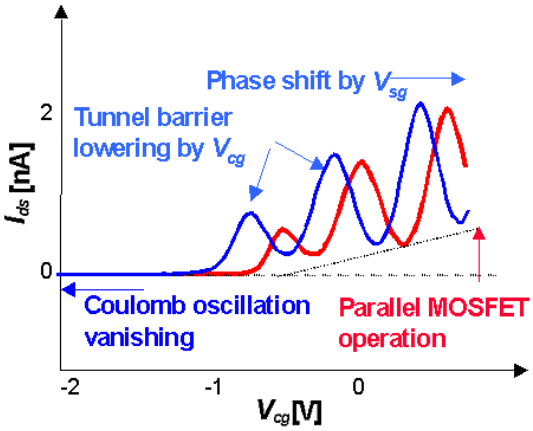

Fig. 2. Typical electrical characteristics of the fabricated SETs. The device with an island size $S_{sg} = 40$ nm was measured at $V_{ds} = 5$ mV and 77 K. Here, V_{cg} and V_{sg} means the biasing voltage for the control gate located on top of the structure and the side gate made by poly-Si sidewall in Fig. 1(a), respectively.

ory, are clearly observed in realistic SETs. First of all, the phase of the Coulomb oscillation is shifted by the sidewall depletion gate voltage (V_{sg}). Secondly, due to the parasitic MOSFET effect the peak-to-valley current ratio (PVCR) decreases as V_{cg} increases [5]. Thirdly, as a result of the tunnel barrier lowering by the V_{cg}, the level of the SET current increases as the control gate voltage (V_{cg}) increases.

The SPICE model for the realistic SET I-V curves was implemented in two parts [6]. The total drain current is given by

$$I_{ds} \cong I_{SET} + I_{MOSFET}, \quad (1)$$

where I_{SET} and I_{MOSFET} are the SET current based on a simple capacitive Coulomb blockade model (*i.e.*, orthodox theory) and a parallel MOSFET current, respectively. The basic formulation for the SET current (I_{SET}) is based on the analytical model proposed by Uchida *et al.* [2]. In addition, the tunnel barrier lowering effect and the phase shift effect of the Coulomb oscillation were included in the I_{SET} [6]. On the other hand, the basic formulation of the parasitic MOSFET (I_{MOSFET}) is based on the SPICE LEVEL 3 MOSFET model, in which the drain current model includes the temperature dependence of both the threshold voltage and the mobility. We have extracted the SPICE model parameters of MOSFETs based on experimental measurements from 4.2 K to 300 K.

The simulation results from our SPICE model were compared with the experimental data from the fabricated SETs. First, the I-V curves of the Coulomb oscillation at various temperatures from our SPICE model were compared with the measured I-V characteristics of the SETs, as shown in Fig. 3(a). The simulation results agree well with the experimental data. Here, it should be emphasized that the parasitic MOSFET effect and the tunnel barrier lowering effect are accurately reproduced in our SPICE model. Secondly, the V_{sg}-dependence of the Coulomb oscillation from our SPICE model was compared with the measured I-V characteristics of the SETs, as shown in Fig. 3(b). The Coulomb oscillation phase shift due to V_{sg} was well reproduced and was in good agreement with the measured data.

III. CMOS/SET HYBRID CIRCUIT SIMULATION

The new SET SPICE model was applied to verify the feasibility of CMOS/SET hybrid multiple-valued logic (MVL) circuits. If the periodic nature of the Coulomb oscillation in SETs is utilized, the CMOS/SET hybrid MVL has potential advantages over binary logic with respect to the number of elements per function and the operating speed [7, 8]. However, previously reported MVL circuits cannot guarantee stable functionality at high temperatures because the peak-to-valley current ratio (PVCR) of the SET degrades due to an increase in I_{MOSFET}. In this work, we propose a new circuit technique in which the MVL can operate at high temperatures and the PVCR of the Coulomb oscillation is prominently decreased.

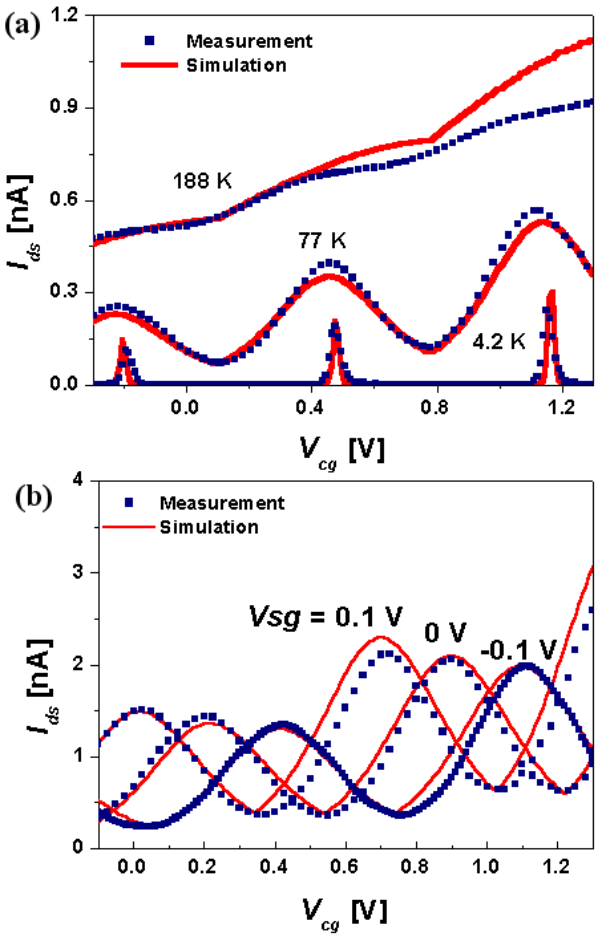

Fig. 3. (a) I-V characteristics of the SETs at various temperatures (V_{ds} = 1 mV) and at various sidewall gate biases at 77 K (V_{ds} = 5 mV).

Figure 4(a) shows a current modulation circuit with a temperature-adaptive biasing scheme, consisting of a constant current source, a MOSFET, and a resistor. The SET drain is biased to V_{gg}-V_{th}, where the voltage V_{gg} is made to trace V_{th} at various temperatures. As a result, the SET drain voltage is kept at a constant voltage. By tuning I_{bias} and R_b, we can adjust this voltage to an optimum value with respect to both the Coulomb blockade condition and the gate-induced transconductance. Too low a voltage to guarantee the Coulomb blockade condition over a wide temperature range leads to a small gate-induced transconductance and inevitably to low performance while too high a voltage to enhance performance may cause a malfunction in the logic at higher temperatures.

Figure 4(b), (c), and (d) show the I_d-V_{cg} characteristic of a SET in the circuit as calculated by using a SPICE simulation. Clear Coulomb oscillations are observed as the gate voltage is changed. A size dependence of the device characteristics is clearly observed at both 27 K and 77 K. The Coulomb oscillation period (ΔV_{cg}) is 210

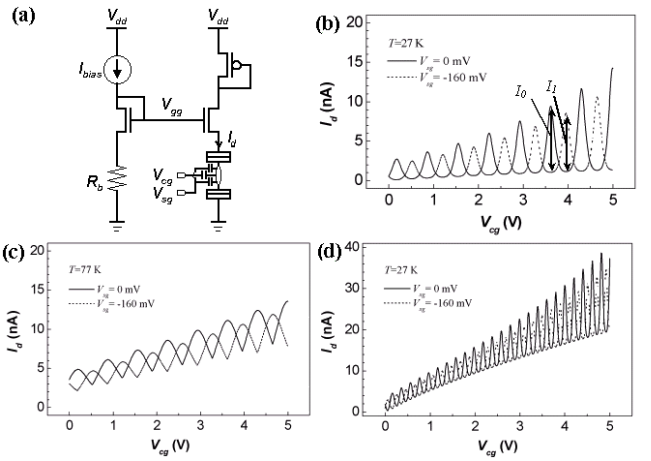

Fig. 4. (a) Schematic diagram of the current modulation circuit incorporated with a temperature-adaptive biasing scheme. A demonstration of the Coulomb oscillation phase shift by applying different voltages to the side gates, V_{even} (= 0 mV) and V_{odd} (= −160 mV) for the cases of (b) S_{sg}= 40 nm at 27 K, (d) S_{sg} = 40 nm at 77 K, and (d) S_{sg} = 90 nm at 27 K. These were calculated using a SPICE simulation.

mV and 675 mV (C_g corresponding to 0.76 and 0.24 aF), respectively, for Si island sizes (S_{sg}) of 90 nm and 40 nm, respectively. Due to the tunnel barrier lowering effect, the off-state leakage current increases as the control gate voltage (V_{cg}) increases. This tendency becomes more conspicuous at higher temperature and larger Si island size. On the other hand, the phases of Coulomb oscillations shifts by π as the side gate voltage changes from V_{even} (= 0 mV) to V_{odd} (= −160 mV). For the application to switching units, these complementary sets of currents deserve special attention because the gap between complementary currents is not diminish by the increasing V_{cg}, the temperature, and S_{sg}.

As a stability-enhanced MVL circuit, we propose a complementary self-biased periodic binary converter. It has been reported that the efficiency of a flash analog-to-digital converter (ADC) can be improved by using periodic binary converters [7]. The previously reported SET/CMOS hybrid periodic binary converter is, however, sensitive to temperature variations because its pull-up load is not adaptive to the pull-down SET current behavior, such as PVCR degradation. Furthermore, SETs with larger quantum islands cannot be utilized because they are more susceptible to temperature variations.

In the suggested scheme, a couple of SETs exhibiting complementary currents, named even mode and odd mode currents, are utilized. Figure 5(a) shows the proposed scheme for a periodic binary converter. The side gate voltages of the SETs, V_{odd} and V_{even}, are biased so that the SET in the biasing stage operates in the odd mode, and the SET in the gain stage operates in the even mode. The pMOSFET current mirror duplicates the complementary current (odd mode current) to the main stage as a current load.

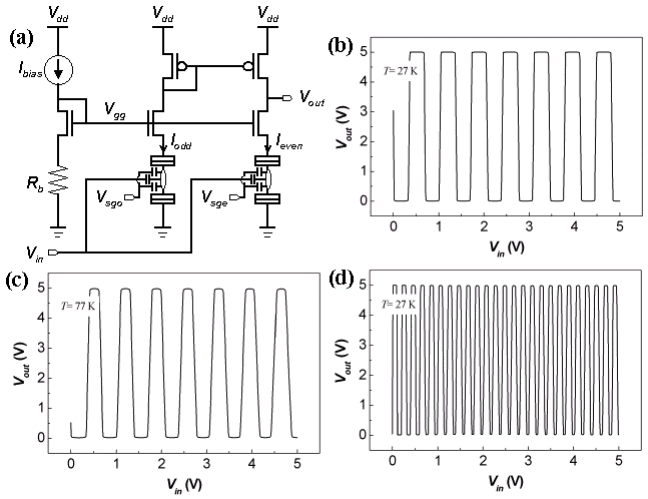

Fig. 5. (a) Schematic of the proposed multiple-valued inverter comprised of a couple of SETs and MOSFETs. The (V_{in}-V_{out}) transfer characteristics for the cases of (b) S_{sg} = 40 nm at 27 K, (d) S_{sg} = 40 nm at 77 K, and (d) S_{sg} = 90 nm at 27 K.

Figure 5(b), (c), and (d) show the (V_{out}-V_{in}) transfer characteristics. The Coulomb oscillations of the SET devices are successfully transformed to voltage signals. As V_{in} is increased, the Coulomb oscillation of the SET produces ouput voltage transitions between the two output states at each cross point of the even and the odd mode currents in Figs. 4(b), (c), and (d). If the even mode current becomes larger than the odd mode current, the output voltage changes to a low-voltage state, and if the odd mode current becomes larger than the even mode current, the output voltage changes to a high-voltage state. Consequently, this switching logic accomplishes the correct function, in principle, if the charging (I_1) and the discharging (I_0) currents shown in Fig. 4(b) are large enough to make a full swing of the output voltage, regardless of the leakage level. As both I_0 and I_1 are increased to more than two times those the previous work, the static noise margin is improved tremendously. Even when the operating temperature was increased to 77 K, where the PVCR of the SET current degrades to as low as 1.7 because of the parasitic MOSFET current induced by tunnel barrier lowering, the switching operation is accomplished successfully. The SET with large island size (S_{sg} = 90 nm) is also observed to exhibit a perfect switching operation thanks to the enhanced static noise margin. Needless to say, a large maximum charging current (I_1) and discharging current (I_0) are helpful for a faster switching operation, as well as for stability enhancement.

IV. CONCLUSIONS

A practical SPICE model for real Si SETs was developed based on a simple analytical model and its appropriate modification. This new SPICE model could reproduce not only the typical Coulomb oscillation of the SETs but also the effects of real SETs, such as the oscillation phase shift due V_{sg}, the tunnel barrier lowering due to V_{cg}, and the parasitic MOSFET effect. This SET SPICE model was successfully applied to a simulation of the characteristics of CMOS/SET hybrid multi-valued logic (MVL) circuits in terms of their stability and performance. We have confirmed that the proposed complementary self-biasing scheme enables the SET/CMOS logic to operate quite well at high temperatures where the peak-to-valley current ratio of the Coulomb oscillation is severely degraded.

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