Complementary Self-Biased Scheme for the Robust Design of CMOS/SET Hybrid Multi-Valued Logic

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Abstract

We propose a new technique to enhance the characteristics of CMOS/SET hybrid multi-valued logic (MVL) circuits in terms of their stability and performance. A complementary self-biasing method enables the SET/CMOS logic to operate perfectly well at high temperature in which the peak-to-valley current ratio of Coulomb oscillation severely decreases. The suggested scheme is evaluated by SPICE simulation with an analytical SET model, and it is confirmed that even SETs with a large Si island can be utilized efficiently in the multi-valued logic. We demonstrate a quantizer implemented by SETs with a 90-nm-long Si island on the basis of measured device characteristics and SPICE simulation, which shows high resolution and small linearity error characteristics.

1. INTRODUCTION

Single-electron transistors (SETs) have attracted much attention due to their potential advantages in implementing multi-valued logic (MVL), utilizing the periodic nature of Coulomb oscillation [1]. However, in order to introduce SETs in practical LSIs, it is essential to increase their operation temperature and develop a new operation scheme of SET/CMOS hybrid circuits.

For the applications of SETs as gate-controlled switching devices in SET/CMOS hybrid circuit, much attention have been paid to meet the requirements for sustaining high peak-to-valley ratio (PVCR) of the Coulomb oscillation of SETs. Most of applications have been achieved under certain conditions such as limited range of temperature and precise control of drain and gate voltage of SET [2][3]. These complicated requirements make the SET circuit design very difficult to be applied in practical use. Therefore, for the design of SET circuits, a methodology is strongly required through which the circuit comes to operate robustly under the low PVCR condition of SETs.

In this paper, we propose a new circuit technique that allows the MVL to operate at high temperatures in which the PVCR of Coulomb oscillation prominently decreases. This technique is based on the usage of a current load whose phase is complementary to that of pull-down current through the SET in an output stage.

Utilizsing the phase shifting nature of Coulomb oscillation current observed in our depletion gate-type SETs which is suitable for a precise control of phase shift, we explain the operation principle of the proposed complementary self-biasing scheme. By SPICE simulation with an analytical SET model, we demonstrate the stability enhancement of the basic MVL components, such as a periodic binary converter and a quantizer.

2. Phase Control of Coulomb Oscillation

Fig. 1(a), (b) shows a schematic diagram and a SEM image of the previously developed Si SET with sidewall depletion gates and (c) shows an equivalent circuit diagram [4]. This device has two electrically induced tunnel barriers and a Si island between them, and shows clear Coulomb oscillation at 4.2~77 K. The island size (S_{sg}) dependence of device characteristics shows good controllability and reproducibility.

However, three physical phenomena distinguished from the orthodox theory are clearly observed in fabricated SETs, as is the case in most of other SETs with a physically formed Si island [5][6]. First of all, the phase of the *Coulomb oscillation* is shifted by the sidewall depletion gate voltage (V_{sg}). Secondly, the peak-to-valley current ratio (PVCR) decreases as V_{cg} increases, due to the parasitic MOSFET effect [7]. Thirdly, the level of the SET current increases as the control gate voltage (V_{cg}) increases, as a result of the *tunnel barrier lowering* by the V_{cg}.

We have developed a physically based analytical model of SET and have confirmed its validity by a comparison with measured characteristics of the fabricated SETs [8]. The SPICE model for the realistic SET *I-V* curves was implemented in two parts.

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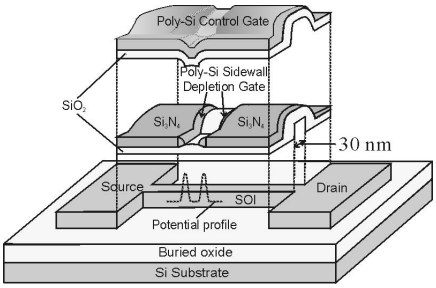

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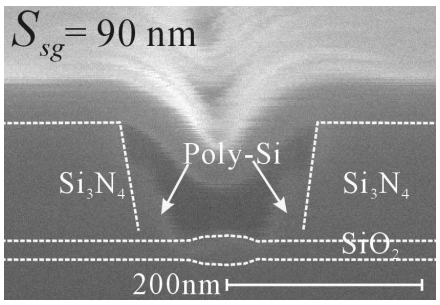

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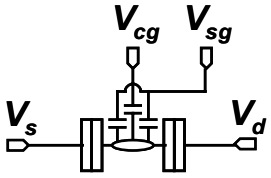


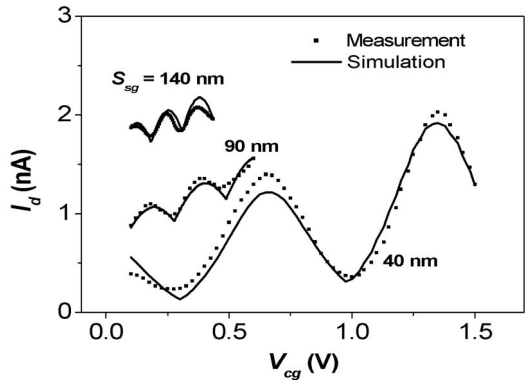
(c)

Fig. 1. (a) Schematic diagram of the SET with sidewall depletion gates on an SOI nano-wire. (b) The SEM image of the fabricated SET with a 90-nm-long Si island. (c) Equivalent circuit diagram.

The total drain current is given by

$$I_{ds} \cong I_{SET} + I_{MOSFET}, \qquad (1)$$

where I_{SET} and I_{MOSFET} are the SET current based on a simple capacitive Coulomb blockade model (i.e., *orthodox theory*) and a parallel-connected MOSFET current, respectively. The basic formulation for the SET current (I_{SET}) is based on the analytical model proposed by Uchida *et al.* [2]. In addition, *tunnel barrier lowering* effect and the phase shift effect of the *Coulomb oscillation* were included in the I_{SET}. On the other hand, the basic formulation of the parasitic MOSFET (I_{MOSFET}) is based on the SPICE LEVEL 3 MOSFET model, where the drain current model includes the temperature dependence of both the threshold voltage and the mobility.



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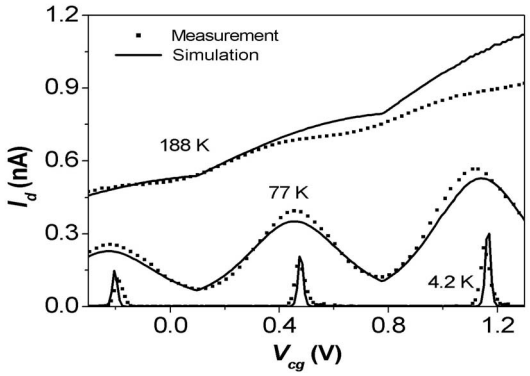

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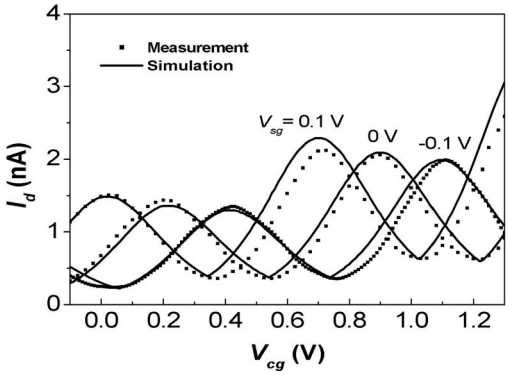

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Fig. 2. Simulated and experimental I_d - V_{cg} characteristics of SETs at various conditions. (a) island size dependence, (b) temperature dependence, and (c) V_{sg} dependence of Coulomb oscillation characteristics, respectively.

Fig. 2 shows the simulated and experimental Coulomb oscillation characteristics of SETs at various island sizes, temperatures and V_{sg}'s. The peak and valley currents of Coulomb oscillations show good agreements between them for various conditions. Moreover, it should be emphasized that V_{sg} dependence of phase shift and V_{cg} dependence of tunnel barrier lowering effect are perfectly represented by the model. We have implemented the SET model into a conventional circuit simulator SPICE, which allows us to verify the feasibility of circuits including SETs.

The phase control of Coulomb oscillation has been employed in logic applications such as CMOS-like SET inverter and multifunctional SET logic [4][10]. However, their application has not fully utilized the multi-peak nature of SET nor made any improvement in terms of stability.

Fig. 3(a) shows a current modulation circuit with a temperature-adaptive biasing scheme, consisting of a constant current source, a MOSFET, and a resistor. The SET drain is biased to V_{gg}-V_{th}, where the voltage V_{gg} is made to trace V_{th} at various temperatures. As a result, the SET drain voltage is kept at a constant voltage. By tuning I_{bias} and R_b, this voltage can be adjusted to an optimum value with respect to both the Coulomb blockade condition and the gate-induced transconductance. Too low voltage for guaranteeing the Coulomb blockade condition over wide temperature range leads to small gate-induced transconductance and inevitably low performance, while too high voltage for enhancing performance may cause malfunction in the logic at higher temperature.

Fig. 3(b), (c) and (d) show the I_d-V_{cg} characteristic of a SET in the circuit calculated by SPICE simulation. Clear Coulomb oscillations are observed along with the gate voltage. The size dependence of the device characteristics is clearly observed at both 27 K and 77 K. The Coulomb oscillation period (ΔV_{cg}) is 210 mV and 675 mV (C_g corresponding to 0.76 and 0.24 aF), respectively, as Si island size (S_{sg}) is varied from 90 nm to 40 nm. Due to the tunnel barrier lowering effect, the off-state leakage current increases as the control gate voltage (V_{cg}) increases. This tendency becomes more conspicuous with the increase of temperature and the Si island size.

On the other hand, it is noticed that the phases of Coulomb oscillations are shifted by π as the side gate voltage changes from V_{even} (= 0 mV) to V_{odd} (= -160 mV).

With regard to a possible application to switching units, these complementary sets of currents deserve special attention because the gap between complementary currents does not diminish by the increase of V_{cg}, temperature and S_{sg}.

3. Complementary Self-Biased Circuits

Two complementary self-biased MVLs are proposed. In these logic circuits, a couple of SETs exhibiting

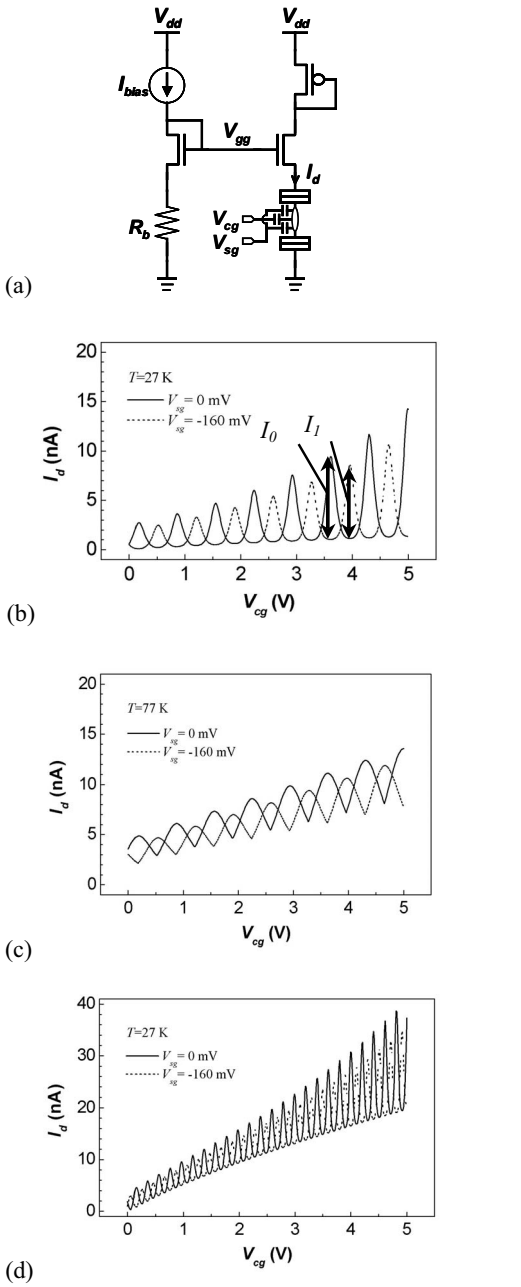


Fig. 3. (a) Schematic diagram of the current modulation circuit incorporated with temperature adaptive biasing scheme. The demonstration of Coulomb oscillation phase shift by applying a different voltage to side gates, V_{even} (= 0 mV) and V_{odd} (= -160 mV) for the case of (b) S_{sg}= 40 nm at 27 K, (d) S_{sg} = 40 nm at 77 K, and (d) S_{sg} = 90 nm at 27 K, respectively. These are calculated by SPICE simulation.

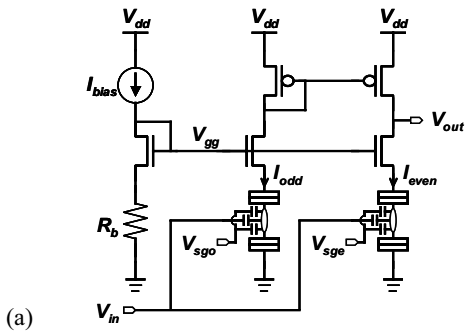
complementary currents, named *even* mode and *odd* mode current, are utilized.

3.1. Periodic binary converter

As a stability-enhanced MVL, we propose a complementary self-biased periodic binary converter. It has been reported that the efficiency of the flash analog-to-digital converter (ADC) can be improved by using a periodic binary converter [1]. The previously proposed SET/CMOS hybrid periodic binary converter called universal literal gate shows sharp transfer characteristics and large output amplitude. However, its functionality is not guaranteed at severe conditions. That is, high temperature and high V_{in} condition can bring about malfunction as the tunnel barrier lowering effect makes the SET valley current to be larger than the constant current load, and thus the switching operation no longer works. For the same reason, similar malfunction may occur if SETs with a larger Si island are used.

Fig. 4(a) shows the proposed scheme for the periodic binary converter, organized by biasing and main function stages. The side gate voltages of SETs, V_{sgo} and V_{sge}, are biased so that the SET in biasing stage operates in odd mode and the SET in gain stage operates in even mode. The pMOSFET current mirror duplicates the complementary current (odd mode current) to the main stage as a current load.

Fig. 4(b), (c) and (d) show the (V_{in} - V_{out}) transfer characteristics. Coulomb oscillations of SET device are successfully transformed to voltage signals. As V_{in} increases, Coulomb oscillation of SET produces ouput voltage transitions between the two output states at each cross point of even and odd mode current in Fig. 3(b), (c) and (d). If the even mode current becomes larger than odd mode current, the output voltage changes to the low voltage state, and if the odd mode current becomes larger than the even mode current, the output voltage changes to the high voltage state. Consequently, this switching logic accomplishes the correct function, in principle, if the charging (I_1) and discharging (I_0) currents shown in Fig. 3(b) are large enough to make a full swing of the output voltage regardless of the leakage level. As both I_0 and I_1 are increased more than two times those in previous work, the static noise margin improves tremendously. Even when the operating temperature rises up to 77 K, where PVCR of SET current degrades as low as 1.7 by the parasitic MOSFET current induced by tunnel barrier lowering, the switching operation is accomplished successfully. It is also observed that the SET with large island size (S_{sg} =90 nm) shows a perfect switching operation thanks to the enhanced static noise margin. Needless to say, a large maximum charging current (I_1) and discharging current (I_0) are helpful for a faster switching operation as well as stability enhancement



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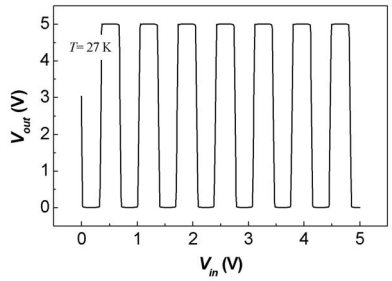

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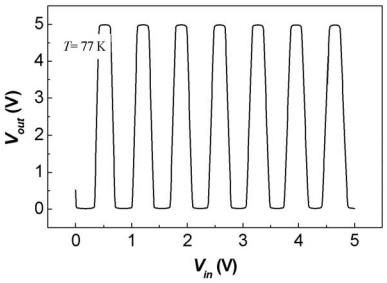

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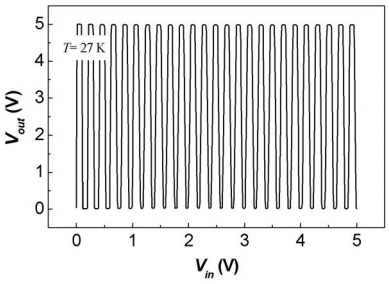

(d)

Fig. 4. (a) The schematic of proposed periodic binary converter comprising of a couple of SETs and MOSFETs. (V_{in} - V_{out}) transfer characteristics for the case of (b) S_{sg} = 40 nm at 27 K, (d) S_{sg} = 40 nm at 77 K, and (d) S_{sg} = 90 nm at 27 K, respectively.

3.2. Quantizer and SRAM

Fig. 5 (a) shows the schematic of a quantizer employing the complementary self-biasing scheme. As the SET control gate and V_{out} is shorted, periodic I_d-V_{cg} characteristics of SETs shown in Fig. 3(d) can be converted into 2-terminal I_d-V_{out} characteristics [1]. With a complementary current load, many stability points appear, and V_{in} fed into V_{out} through the transfer gate is quantized to a stability level after the gate is cut off.

Quantization operation is demonstrated in Fig. 5(b). A triangular wave is fed to V_{in}, and the gate of the transfer MOSFET is driven by short pulses of a clock. V_{out} is determined by V_{in} at the sampling moment, and remains between sampling operations. This self-latching characteristic helps simplifying digital circuit systems by removing additional latching elements. The resolution of quantization is proportional to the number stability points. When SETs with a 90 nm Si island are used, V_{out} is quantized to 16 levels at 3.2V supply voltage, which correspond to the number of stability points in Fig. 3(d). This is the highest resolution among the SET/CMOS hybrid quantizer circuits previously reported. It is obvious that the improvement of resolution is due to the static noise margin enhancement of the proposed biasing scheme. Both the maximum differential nonlinearity (DNL) and integral nonlinearity(INL) errors are measured to be less than ± 0.1 LSB.

Both self-latching and small nonlinearity error characteristics are the key requirements for multi-level storage memory. Fig. 6 shows a schematic diagram of seven-transistor multi-level static memory cell based on the proposed quantizer. As a practical design, depletion mode grounded-gate nMOSFETs, **M1** and **M2**, are used to sustain the SET drain voltage around the absolute threshold voltage of the two transistors. Each side gate of the two SETs, $\mathbf{S_o}$ and $\mathbf{S_e}$, is connected to the drain of **M4** and ground, respectively, so that the phase difference between the drain currents of two SETs is tuned to π by the threshold voltage adjustment of pMOSFETs **M4** and **M5**. The pass transistor **M3** controls the access to the cell. If a 16-level storage cell is used, the memory density can be increased by about four times. The data sensing speed and dynamic noise margin during read operation can be enhanced by employing a storage capacitor and current-mode sensing scheme [11].

4. Conclusions

By SPICE simulation with an analytical SET model, we demonstrate the stability enhancement of the basic MVL components, such as periodic binary converters and a quantizer. We have confirmed that the proposed complementary self-biasing scheme enables the SET/CMOS logic to operate quite well at high temperatures in which the peak-to-valley current ratio of Coulomb

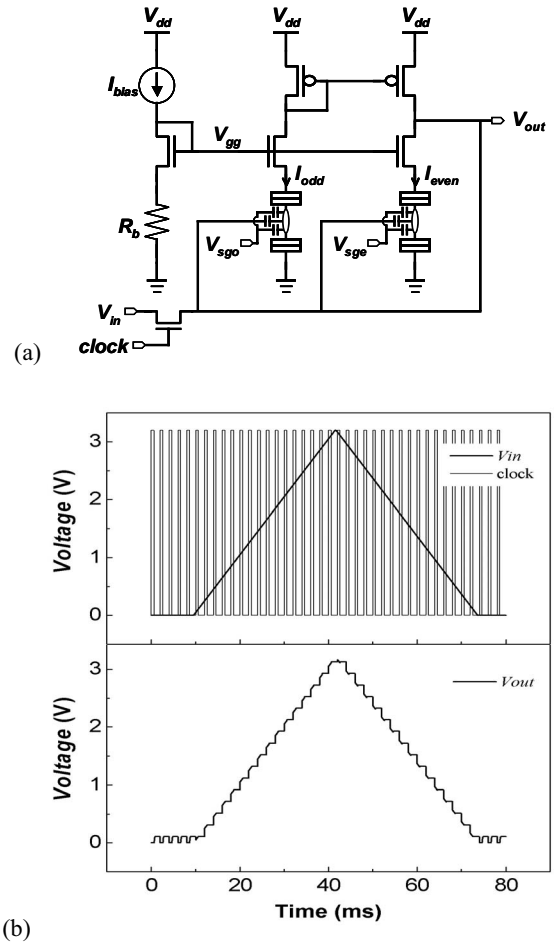

Fig. 5. (a) The schematic of a quantizer employing complementary self-biasing scheme, (b) input, clock and quantized V_{out} voltage.

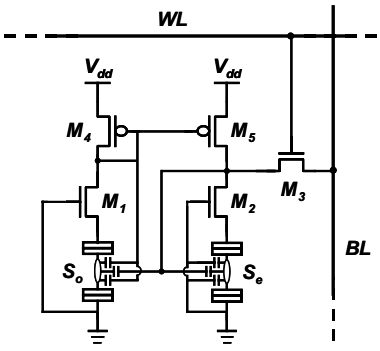

Fig. 6. The schematic diagram of a multiple-level single-electron static memory cell with five MOSFETs.

oscillation severely degrades. In principle, their functionality is guaranteed if only the swing of Coulomb oscillation is sufficient regardless of the leakage, even at more or less low PVCR conditions. Even SETs with a large Si island, which have been difficult to use due to low switching performance, can be utilized efficiently in multiple-valued circuits such as a quantizer and a multi-level static memory cell.

Acknowledgement

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