Realistic Single-Electron Transistor Modeling and Novel CMOS/SET Hybrid Circuits

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***Abstract*— A practical single electron transistor (SET) model has been proposed with appropriate modifications to the previous analytical model. We have observed that non-ideal SET current behaviors such as turn-off and peak-to-valley ratio(PVCR) degradation is successfully reproduced by the new SET model. Based on the realistic SET model, we have developed a novel circuit scheme which enhances the stability of CMOS/SET hybrid logic. It is demonstrated that a universal literal gate with complementary self-biasing scheme operates quite well at high temperature in which the peak-to-valley current ratio of Coulomb oscillation degrades severely.**

Keywords- single eletron transistor(SET); modeling; stability; hybrid; multiple-valued logic(MVL)

I. INTRODUCTION

Recently, macro-model and analytical SET model have been proposed for circuit simulation [1,2]. However, in order to design SET circuits practically, we need a realistic model which is validated by actual experimental data not by Monte Carlo simulation results. So it is very important to develop a physically based SET model, which reflects both ideal and non-ideal characteristics of SETs accurately for wide range of temperature and bias conditions.

Previously reported SET applications have been achieved under limited temperature range [3]. However, in order to introduce SETs in a practical system, a new design concept is required so as to enlarge the operating temperature range. The realistic SET model is expected to play an important role in the development of stable SET circuits.

In this paper, we propose a design methodology to enhance the stability of CMOS/SET hybrid circuits. We have confirmed the feasibility of the suggested methodology by checking the performance improvement of a universal literal gate which utilizes the proposed scheme.

II. MODELING

Fig. 1 shows a schematic diagram of the previously developed Si SET with sidewall depletion gates. An electrically induced quantum dot is formed in the 30nm-wide channel of the SOI MOSFET by the field effect of the sidewall gate bias(V_{sg}). The potential of the quantum dot is controlled by the control gate bias(V_{cg}). Previously, we have reported an empirical SET modeling which shows good agreement with experimental data in terms of Coulomb oscillation period, phase shift, and parasitic MOSFET operation [4]. In this work, focuses are on the current turn-off behavior and more elaborate modification to tunnel barrier lowering effect as a function of temperature, quantum dot control voltage(V_{cg}) and tunnel barrier control voltage(V_{sg}), which have been observed in recently reported SETs formed on Si nano-structures [5,6].

Experimental observations indicate that the SET threshold voltage shows non-linear dependency on temperature variation as shown in Fig. 2, contrary to that of MOSFET which shows linear dependency [7]. As temperature increases from 4.2K to 300K, a large shift of –15mV/K in threshold voltage has been observed around 77K~188K. In order to gain a better understanding of the physical mechanism responsible for this unusual phenomenon, a detailed characterization study has been carried out.

Fig. 3 shows an equivalent circuit diagram of the fabricated device, which is composed of an SET and five parasitic MOSFETs; one is parallel-connected to the SET and the other four are connected serially.[4] We have modeled the turn-off characteristics as serial barrier MOSFETs, M2 and M4, outsides of SET in which effective gate voltage is obtained by weighted summation of V_{cg} and V_{sg} corresponding to the dielectric thickness [6]. The drain current can be expressed as

$$I_{d\_M2,M4} = CAL \cdot \mu(T)\{\alpha \cdot V_{cg} + \beta \cdot V_{sg} - V_{th}(T)\} \quad (1)$$

$$\mu(T) = U_0 \cdot (T/300)^{BEX} \quad (2)$$

$$V_{th}(T) = V_{to} + (\gamma \cdot T + \delta \cdot T^2) \cdot (k_B/q) \quad (3)$$

where α and β are weighting parameters, γ and δ are fitting parameters for the modeling of non-linear shift of threshold voltage.

The basic formulation of the core SET current is based on the analytical model proposed by Uchida et al. [2]. To take tunnel barrier lowering effect into account, we have introduced modulation factor to the tunneling resistance R_T. Since the tunneling resistance is determined by the shape of the potential barrier, the modulation factor is a function of V_{cg} and V_{sg},

$$R_T = R_{T0} \exp(\chi \cdot V_{cg} + \kappa \cdot V_{sg}) \quad (4)$$

where χ and κ are fitting parameters. The simulation result from the modified SET model was compared with the

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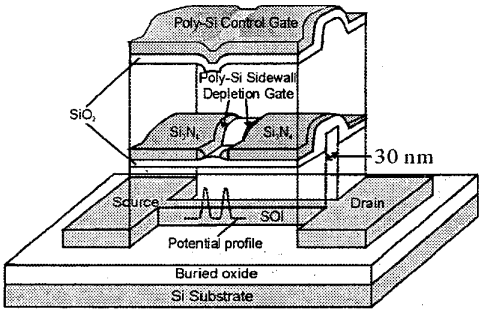

Figure 1. Schematic diagram of the fabricated single electron transistor.

experimental data of the fabricated SET.

Fig. 4 shows that non-ideal SET current behavior such as turn-off and tunnel barrier lowering induced PVCR degradation along the V_{cg} are accurately reproduced for wide range of temperature. Fig. 5 shows phase shift characteristics for some V_{sg} changes. It is also observed that tunnel barrier lowering and turn-off characteristics along the V_{cg} are accurately reproduced at various V_{sg}'s.

The developed SET model is expected to be very useful in practical SET circuit design, since it reflects both ideal and non-ideal characteristics of SETs accurately for wide range of temperature and bias condition.

III. CIRCUIT APPLICATION

By the SPICE simulation employing the developed SET model, we propose a novel circuit scheme to enhance the stability of CMOS/SET hybrid logics in real world.

Fig. 6 shows CMOS/SET hybrid current modulation circuits for complementary self-biased multiple-valued logic. Each circuit is composed of a PMOS and a NMOS field effect transistor and a SET. For the phase control of SET currents, side gate bias voltages(V_{sg}'s) are self-generated without external bias. Odd mode current is made by biasing V_{dd} minus PMOS threshold voltage to the SET side gate, while even mode current is made by zero volt biasing to SET side gate. By adjusting V_{dd} level and PMOS threshold voltage, a complementary pair of current can be obtained. Here, NMOS transistor M_1 and M_2 are depletion mode transistors for the appropriate biasing for SET drains.

The SET valley current increases as V_{cg} increases by the tunnel barrier lowering effect. This tendency becomes more conspicuous at higher temperature as shown in Fig. 6. However, it is noticed that the complementary relationship between the two currents, I_{odd} and I_{even}, does not change at both cases.

Due to the periodic nature in V_{cg}-I_{ds} characteristics, SETs have attracted much attention for their potential advantages in implementing multiple-valued logic. Actually, some SET-based universal literal gates have been proposed, as basic components of the multiple-valued logic.[8,9]

However, the previously reported scheme cannot guarantee the stable operation at high temperature, and needs extra bias. Fig. 7 shows a schematic diagram of a self-biased universal literal gate, and its transfer characteristics. Two current modulation blocks in Fig. 6 are combined so as to utilize the differential amount of the complementary currents, which does not diminish due to the increase of V_{cg} and

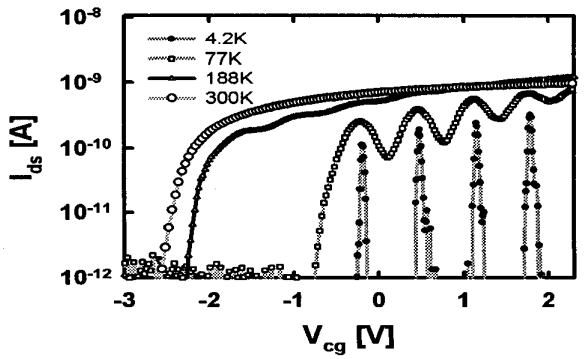

Figure 2. Turn-off characteristics of SET current for various termperatures.

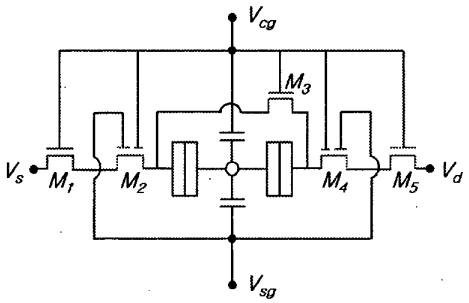

Figure 3. Equivalent circuit model of SET.

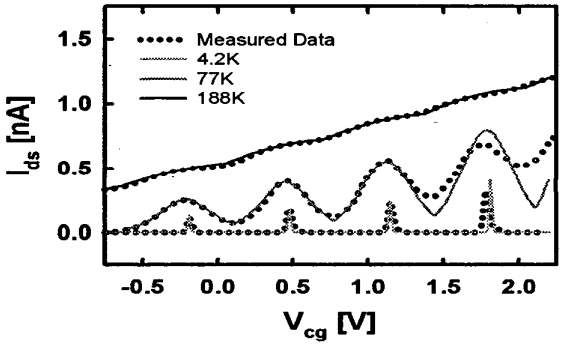

Figure 4. I-V characteristics for various temperatures at V_{ds}=1mV

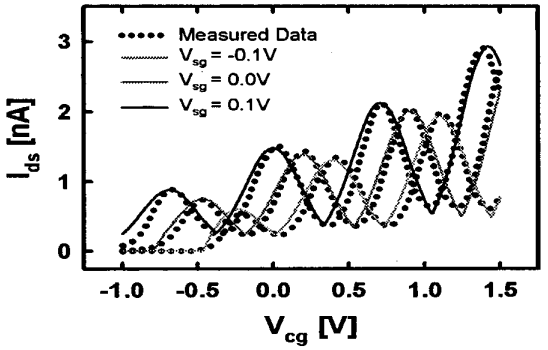

Figure 5. Phase shift characteristics for the V_{sg} variations at V_{ds}=5mV

temperature. As a current load, the PMOS current mirror, M_5, duplicates the complementary current to the output stage. In principle, if only the difference between I_{odd} and I_{even} is large enough, this switching logic carries out a correct function regardless of the leakage level of the SET valley current. Consequently, this scheme is more immune to temperature variation, and guarantees stable operation over wide range of input voltage. As shown in voltage transfer characteristics, even when the operating temperature rises up to 77K, the switching operation is accomplished successfully. Needless to say, this differential mode processing is helpful for a faster switching operation as well as stability enhancement.

IV. SUMMARY

A realistic SET model has been developed, which reflects both ideal and non-ideal characteristics of SETs accurately for wide range of temperature and bias condition. Based on the practical SET model, we have developed a design methodology which enhances the stability of the circuits. It is demonstrated that a CMOS/SET multiple-valued logic with complementary self-biasing scheme operate quite well at high temperature in which the peak-to-valley current ratio of Coulomb oscillation degrades severely.

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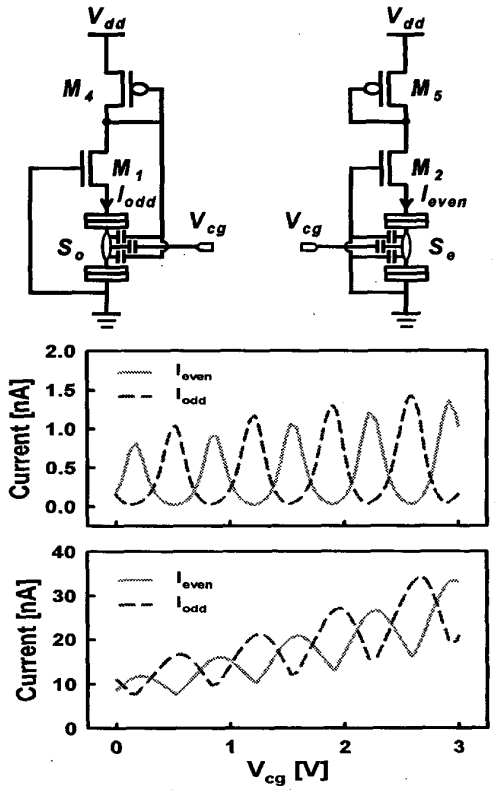

Figure 6. CMOS/SET hybrid current modulation circuits for generating complementary currents and their I-V chracteristics.

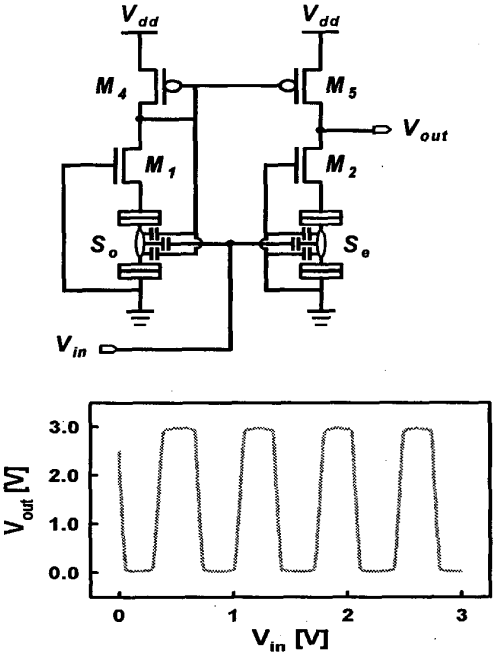

Figure 7. A universal literal gate implemented by complementary self-biased scheme and its transfer chracteristic