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Single-electron transistors fabricated with sidewall spacer patterning

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Abstract

We have implemented a sidewall spacer patterning method for novel dual-gate single-electron transistor (DGSET) and metal–oxide–semiconductor-based SET (MOSET) based on the uniform SOI wire, using conventional lithography and processing technology. A 30 nm wide silicon quantum wire is defined by a sidewall spacer patterning method, and depletion gates for two tunnel junctions of the DGSET are formed by the doped polycrystalline silicon sidewall. The fabricated DGSET and MOSET show clear single-electron tunneling phenomena at liquid nitrogen temperature and insensitivity of the Coulomb oscillation period to gate bias conditions. On the basis of the phase control capability of the sidewall depletion gates, we have proposed a complementary self-biasing method, which enables the SET/CMOS hybrid multi-valued logic (MVL) to operate perfectly well at high temperature, where the peak-to-valley current ratio of Coulomb oscillation severely decreases. The suggested scheme is evaluated by SPICE simulation with an analytical DGSET model, and it is confirmed that even DGSETs with a large Si island can be utilized efficiently in the multi-valued logic.

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1. Introduction

Single-electron tunneling through a quantum dot is a prominent and ubiquitous phenomenon in mesoscopic systems. Single-electron transistors (SETs) utilizing this

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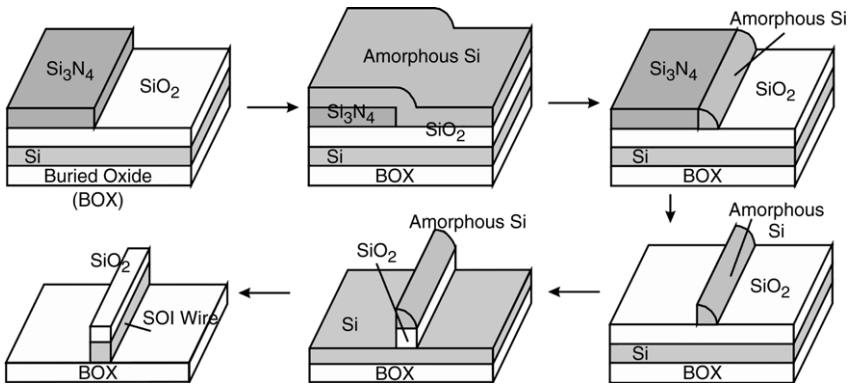


Fig. 1. A schematic diagram of the process sequence of the sidewall spacer patterning method.

phenomenon have been extensively studied for application to ultra-large-scale integrated circuits, due to their high integration density and low power consumption. The operation temperature of silicon-based SETs has been increased to room temperature [1, 2], and their application to logic circuits operating at 20 K has been reported [3]. Reproducible fabrication technology and controllable device characteristics, however, are still a target pursued by many researchers, and it is worthwhile to consider the reproducible structure of Si-based SETs whose electron transport is controlled by a geometrically well-defined Si island.

In this paper, we present a promising SET structure based on silicon-on-insulator (SOI) quantum wires and a geometrically well-defined island beyond the limit of lithography resolution, fabricated by a *sidewall spacer patterning* method. On the basis of the phase control capability of the sidewall depletion gates, we have proposed CMOS/SET hybrid multi-valued logic (MVL) circuits and confirmed the operation of a universal literal gate at 77 K, using SPICE modeling and simulation.

2. Sidewall spacer patterning

Fig. 1 shows the process sequence of the sidewall spacer patterning method. It consists of six major steps. After an oxide layer is deposited on an SOI layer, a nitride layer is deposited and patterned by conventional photolithography. Then, amorphous silicon is deposited and annealed, so that the edge of the nitride layer is fully covered. The amorphous silicon layer is anisotropically etched until the whole layer is removed except the sidewall spacer (the part at the edge corner of the nitride layer). This amorphous silicon strip serves as an etch mask for the definition of the Si quantum wire. The subsequent chemical etching of the nitride and anisotropic etching of the oxide and Si form a Si quantum wire.

Fig. 2 shows the scanning electron microscope image of a patterned Si wire obtained by the sidewall spacer patterning method. Very uniform 30 nm wide Si wires with no irregularities can be created by this method [4].

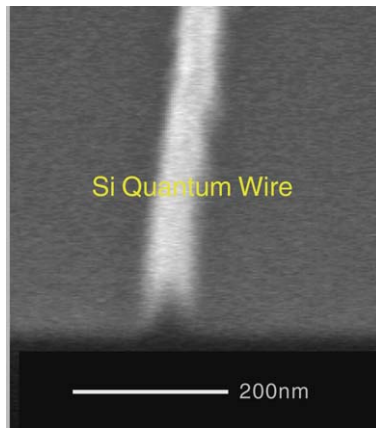


Fig. 2. The SEM image of an SOI quantum wire patterned by the sidewall spacer patterning method.

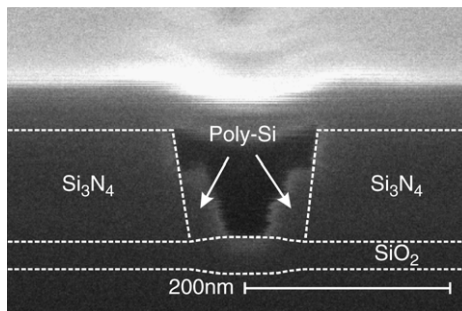


Fig. 3. The SEM image of the cross-section of the fabricated dual-gate SET.

3. Dual-gate single-electron transistor (DGSET)

A dual-gate single-electron transistor (DGSET) based on a Si quantum wire has a Si island electrostatically defined by two polycrystalline silicon (poly-Si) sidewall depletion gates, which wrap the quantum wire in order to control the potential within the Si quantum wire (Fig. 3). The final width of the SOI wire W_{ch} and the separation between the two sidewall gates S_{sg} are controlled to be 23 nm and 37 nm, respectively.

Fig. 4 shows a schematic diagram of the fabricated device. The electron channel in the Si wire is induced by the back-gate bias, V_{bg} . Two tunnel barriers are induced by the bias of the poly-Si sidewall depletion gates, V_{sg} , and the potential in the Si island is controlled by the bias of the top control gate, V_{cg} .

Fig. 5(a) shows the drain current, I_{ds} , measured at 77 K as a function of V_{cg} and the drain–source voltage, V_{ds} . The Coulomb gap is clearly modulated by V_{cg} . Clear equidistant Coulomb oscillation peaks ($\Delta V_{\text{cg}} = 675$ mV) can be seen in the $I_{\text{ds}}-V_{\text{cg}}$ curves (Fig. 5(b)). From the oscillation period, the effective size of the quantum dot is estimated to be smaller

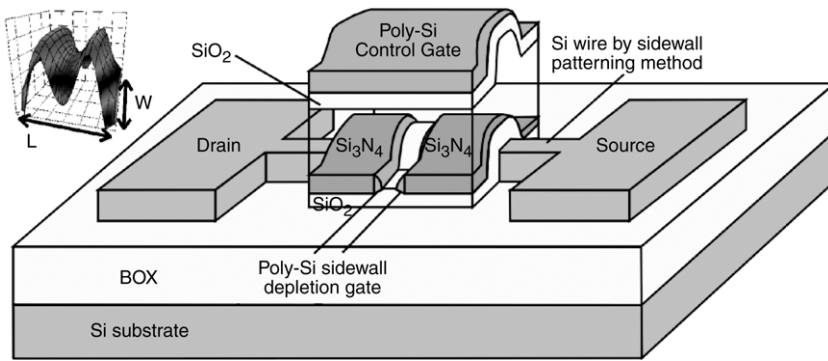


Fig. 4. A schematic diagram of the fabricated dual-gate single-electron transistor structure.

than the geometrically defined dimension of the island ($W_{\text{ch}} \times S_{\text{sg}}$), which is effectively shrunk by the field effect of V_{sg} .

Fig. 6 shows the $I_{\text{ds}}-V_{\text{cg}}$ curves as a function of V_{sg} at 77 K. At a fixed V_{sg} , a ΔV_{cg} of 675 mV is maintained in sweeping V_{cg} [5]. This confirms the stability of the Coulomb oscillation for different depletion gate biases. In addition, a significant amount of phase shift in the Coulomb oscillation is observed as a function of the side-gate voltage, V_{sg} , and this phenomenon can be very useful in circuit application.

4. MOS-based single-electron transistor (MOSET)

SOI MOSFETs with a degenerately doped body can be operated as a SET (Fig. 7(a)) when the channel size shrinks down to the mesoscopic regime. Degenerate doping in the channel and source/drain enables band-to-band tunneling which can play a major role in the transport between the channel and source/drain. Under these conditions, degenerate p^+-n^+ tunnel barriers and a 30 nm square channel defined by the sidewall spacer patterning method act as tunneling barriers and a Si island in a SET, respectively. This structure is based on the conventional MOSFET, so the name ‘MOSET’ (MOS-based SET) is derived. Fig. 7(b) shows the $I_{\text{ds}}-V_{\text{gs}}$ characteristics at 77 K. In the case of the MOSET, clear Coulomb oscillations are observed in the drain current, while they are not observed for a MOSFET as shown in the inset of Fig. 7(b). There are three primary peaks, whose number is limited by the finite number of available energy states in the valence band. The gate voltage spacing (ΔV_{gs}) between these peaks is about 220 mV and this is consistent with the device dimensions. These characteristics confirm single-electron charging effects based on band-to-band tunneling [6].

5. Multi-valued logic circuit application

On the basis of a SPICE simulation employing a DGSET model, we propose a novel circuit scheme for enhancing the stability of CMOS/SET hybrid multi-valued logic (MVL) [7]. Fig. 8(a) and (b) show a schematic diagram of a complementary self-biased

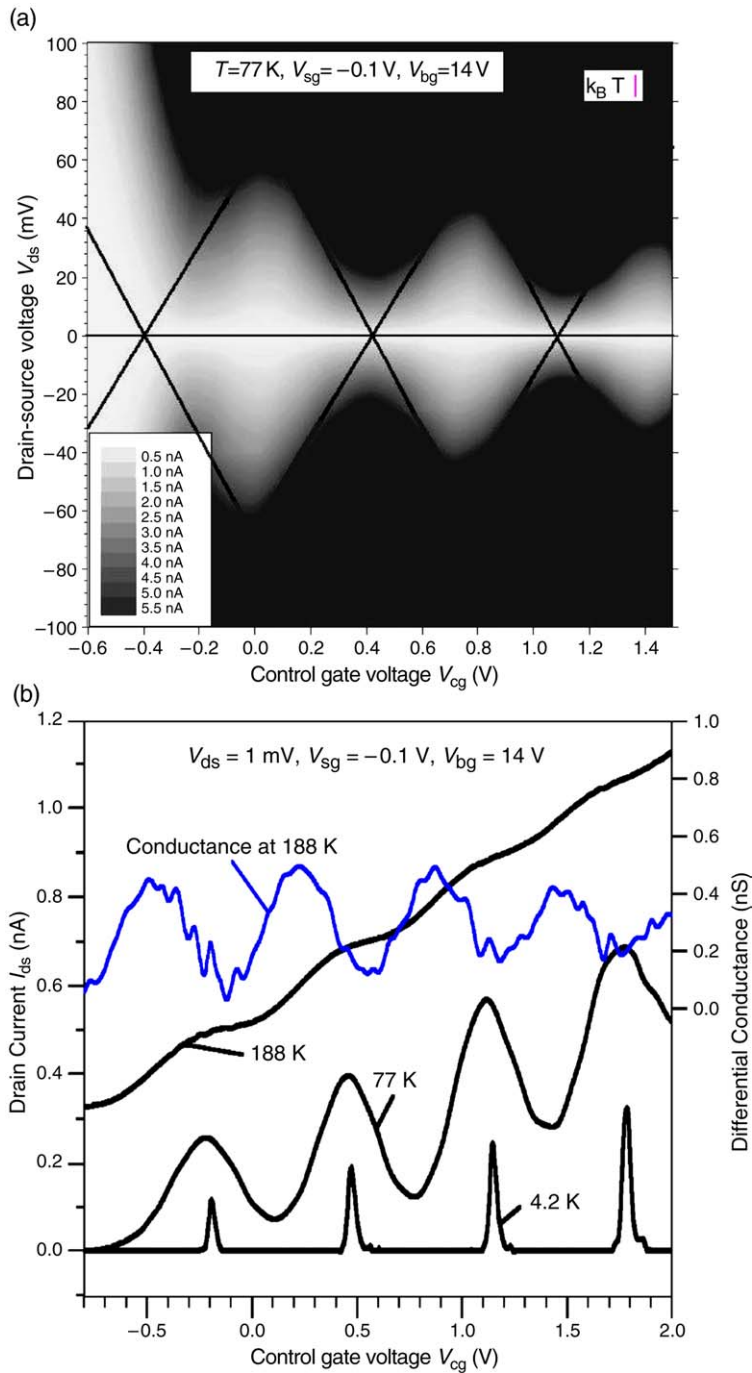


Fig. 5. Characteristics of the fabricated dual-gate single-electron transistors: (a) a contour plot of the drain current I_{ds} as a function of V_{cg} and V_{ds} at 77 K; (b) I_{ds} - V_{cg} characteristics as a function of the temperature.

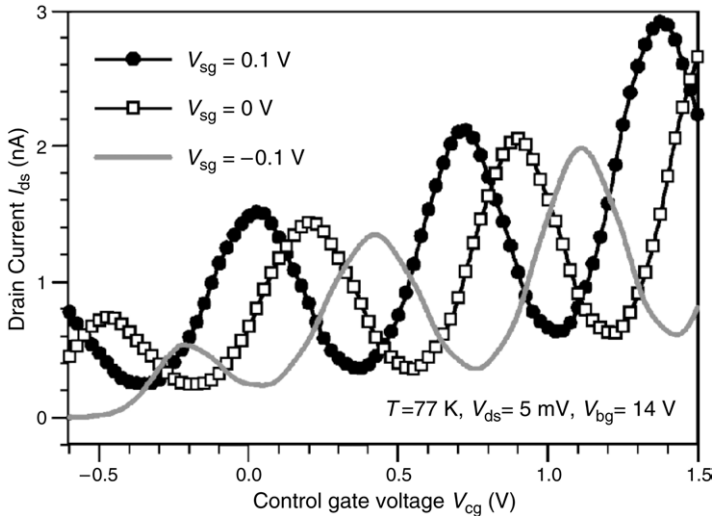


Fig. 6. I_{ds} - V_{cg} characteristics as a function of the depletion gate bias V_{sg} at 77 K. The stability of the Coulomb oscillation period and the controllability of the phase shift are clear.

universal literal gate and its transfer characteristic. Two CMOS/SET hybrid current modulation blocks are combined so as to utilize the difference of the complementary currents generated by the phase shift. The p-channel MOSFET (pMOSFET) current mirror, M_5 , duplicates the complementary current to the output stage. If the difference between the currents of two current modulation blocks is large enough, this switching logic carries out the correct function regardless of the leakage level of the SET valley current. Consequently, this scheme is more or less immune to temperature variation, and guarantees stable operation over a wide range of input voltage. As shown in the voltage transfer characteristic, the switching operation is accomplished successfully at 77 K. This differential mode processing is helpful for a faster switching operation as well as stability enhancement.

6. Conclusion

We have implemented a *sidewall spacer patterning* method for SETs based on the uniform SOI wire, using conventional lithography and processing technology. The fabricated DGSET and MOSET show clear single-electron tunneling phenomena at liquid nitrogen temperature due to the definite formation mechanism of tunnel junctions and the Si island, and have merit for near-future application in integrated CMOS/SET hybrid circuits, since all the fabrication technologies are compatible with the conventional Si CMOS technology. For the effective utilization of the periodic oscillatory nature in SETs, we have developed a complementary self-biased scheme applicable to the MVL circuit, enhancing the stability of the circuit operation at high temperature. A universal literal gate based on this scheme shows excellent characteristics at 77 K, where the peak-to-valley current ratio of an SET is degraded significantly.

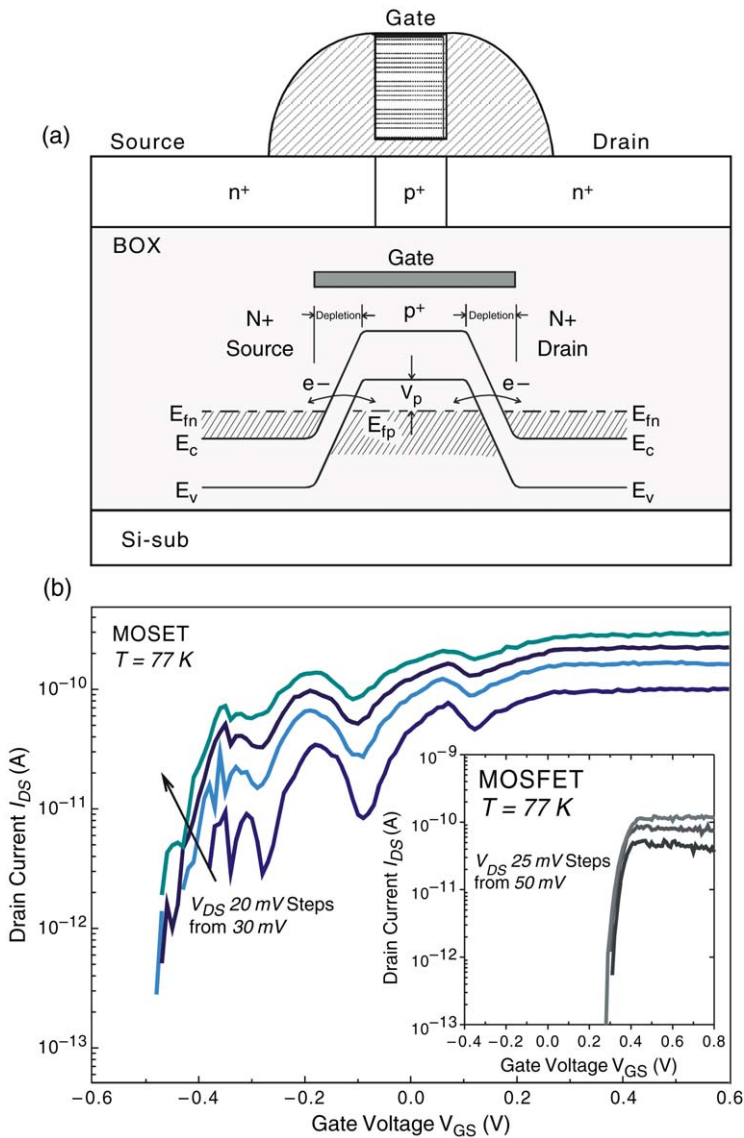


Fig. 7. (a) A cross-sectional schematic diagram of the fabricated MOSET and the energy band diagram. (b) I_{ds} - V_{gs} characteristics of fabricated devices at 77 K. (A comparison between the MOSET and MOSFET in a log-scale plot of the drain current I_{ds} .)

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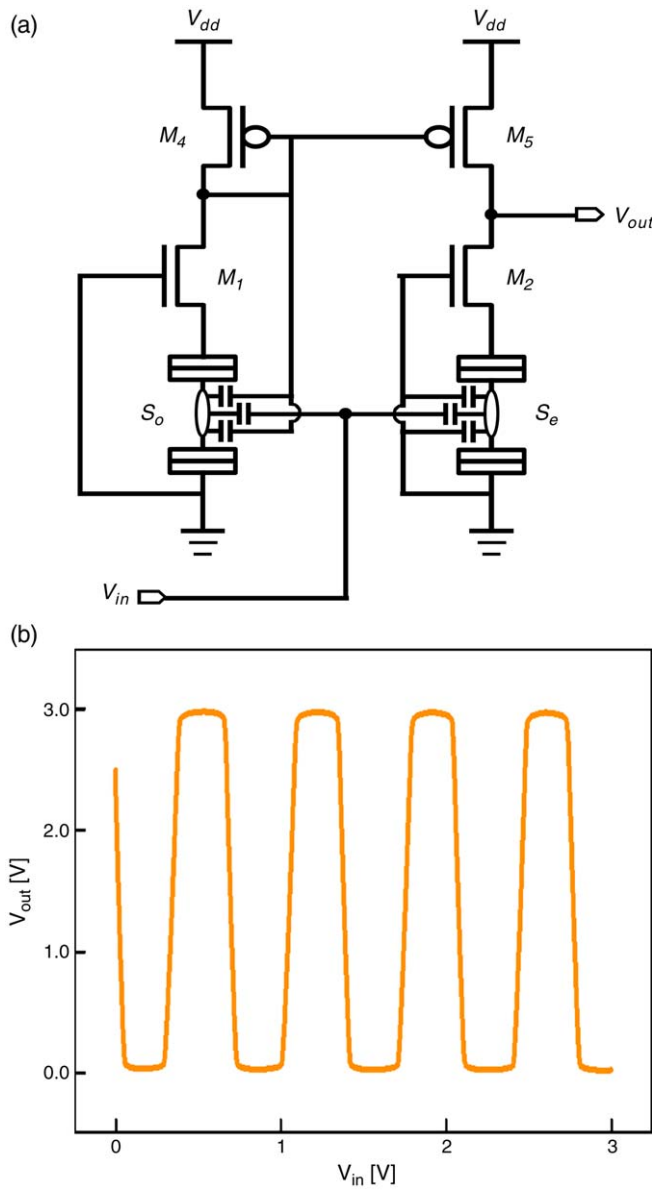


Fig. 8. (a) A universal literal gate implemented by a complementary self-biased scheme and (b) its transfer characteristic at 77 K. Despite the severe degradation in the peak-to-valley current ratio of the SET, the output voltage shows a full swing.

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